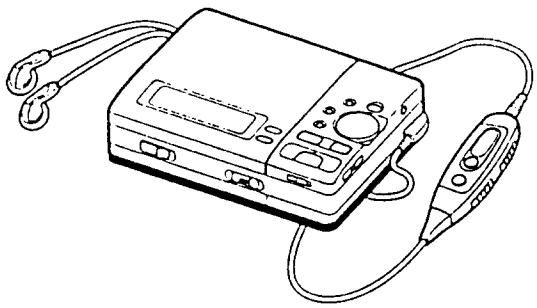
MZ-R3

OPERATION MANUAL



PORTABLE MINIDISC RECORDER

SONY®

TABLE OF CONTENS

I. 3RD GENERATION PORTABLE MD

1. Outline

(1) 3rd Generation MD

Portable MDs are divided into different "Generations" according to the main ICs used for their circuits. The recording and playback types and playback only types have almost the same circuit design. The playback only type just does not have a recording function.

The 1st generation is incorporated with two ATRAC processing ICs for its left and right channels. The 2nd generation has only one ATRAC processing IC.

The 3rd generation, due to the incorporation of a digital servo, is equipped with only one IC for performing both digital signal processing (DSP) and servo processing (SSP). Its shock-proof memory control IC and ATRAC processing IC has also been integrated into one. (Refer to Outline of Circuits for details.)

The 3rd generation MD models available are;the recording/playback MD MZ-R3 marketed in 1995, the recording/ playback MD for business use with built-in mic and speaker MZ-B3, and the playback only MD MZ-E3.

	Recording/Playback Unit	Playback Only Unit
1st Generation	MZ-1, ZS-M1	MZ-2P
2nd Generation	MZ-R2	MZ-E2
3rd Generation	MZ-R3, MZ-B3	MZ-E3

Table 1-1-1. MD Generations and Models

(2) MZ-R3 Features

- Up to 148 minutes of monaural recording
- Digital recording from optical mini input terminal (44.1 kHz only)
- Character input is simple with use of rotating dial
- Track editing by Track-marking function and MOVE function
- Position pointer which shows at a glance the remaining space of the disc and current position.
- Automatic recording of date of recording

(3) MZ-B3

- Up to 148 minutes of monaural recording
- Extended playback (3 AA type alkaline batteries can be loaded)
- Built-in monaural mic and speaker
- Digital VOR function which starts/stops recording according to the sound
- 2 types of fast listening playback
- Position pointer which shows at a glance the remaining space of the disc and current position.
- Stereo recording by external stereo mic

(4) MZ-E3

- Built-in small liquid crystal display for checking track number.
- Liquid crystal remote control headphone which shows song name
- Monaural mode playback

<Function>	MZ-B3	MZ-R3	MZ-E3
Recording/playback	Recording/Playback	Recording/playback	Playback only
Playback VOL	Rotating mechanism method	Electronic VOL	Electronic VOL
Remote Controller	×	Remote controller	LCD remote controller
Headphone Output	○	○	○
Line Output	×	○	×
Digital Output	×	×	×
Line Input	×	○	×
Digital Input	×	○	×
Mic Input	○ (Built-in monaural/ external stereo)	○ (External stereo)	×
AVLS	×	○	○
DBB	×	○	○
RESUME	○ (Always ON)	○ (Always ON)	○ (Always ON)
Beep Sound	×	○	○
Recording Method	AGC only	AGC or MANUAL	×
Monaural Recording	○	○	×
Monaural Playback	○	○	○
Automatic Track mark	×	○ (2 seconds no sound)	×
Fast Listening Playback	○	×	×
Character Input	×	○	×

Table 1-1-2. Comparison of 3rd Generation MD Functions

<Power Supply>	MZ-B3	MZ-R3	MZ-E3
AC adapter	AC-E45L (4.5V, 500mA)	AC-E455 (4.5V, 500mA)	AC-E455 (4.5V, 500mA)
Built-in Alkaline Battery	Three	Two	Two
Built-in Battery (Ni-MH)	×	BP-DM20 (2.4V)	BP-DM20 (2.4V)
External battery (LI-Ion)	LIP-12 (3.6V)	LIP-12 (3.6V)	LIP-12 (3.6V)
Ni-MH battery charging function	×	○	○
Li-Ion battery charging function	×	×	×
Backup battery for clock	MnO_2-Li	MnO_2-Li	×

Table 1-1-3. Comparison of 3rd Generation MD Power Supplies

	Continuous Recording	Continuous Playback
Ni-MH battery	Approx. 2 hours	Approx. 3 hours
Alkaline AA dry batteries	Approx. 2 hours	Approx. 4 hours
Li-Ion rechargeable batteries	Approx. 2.5 hours	Approx. 4 hours
Alkaline type AA dry batteries+Li-Ion rechargeable batteries	Approx. 4.5 hours	Approx. 8 hours
Ni-MH rechargeable batteries+Li-Ion rechargeable batteries	Approx. 4.5 hours	Approx. 7 hours

Table 1-1-4. MZ-R3 Recording/Playback Time

2. New Functions

(1) Recording Functions

(i) Monaural Recording

The MZ-R3 is capable of recording in the monaural mode. In the monaural mode, recording time is twice that of the stereo mode and up to 148 minutes of recording is possible on one disc (MDW-74).

In the monaural mode, both the Lch and Rch sounds are recorded together in analog recording while only the Lch sound is recorded in digital recording.

The monaural mode serves as the standard of MDs, but the first and the second generational MDs are not equivalent to playing back in the monaural mode on general principles*. Exceptionally, MDS-501 (the second generational home-type MD player) can be output the played back sound in the monaural modes.

*Output the played back sound in the monaural mode

Some of the first and the second generational MDs (MZ-R2 etc.) can be output the played back sound in the monaural mode.

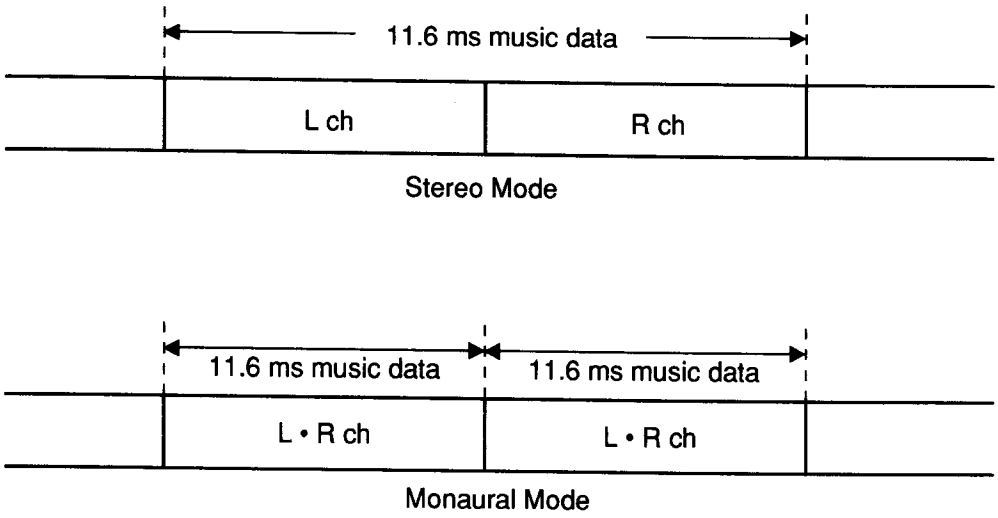


Figure 1-2-1. Monaural Mode Data Structure

The disc rotation speed and data reading method in the monaural mode is the same as the stereo mode. 0.5 seconds of read data (1 cluster) is equivalent to about 2 seconds of music data in the stereo mode, and to about 4 seconds of music data in the monaural mode. As twice the data of the stereo mode is read in the monaural mode, its shock-proof efficiency has also been doubled (above 20 seconds).

(Note)Monaural Mode Recording

Monaural recording in MZ-R3 means recording in the monaural mode. Therefore, even if the monaural mic is connected, unless the monaural mode is switched on, recording will only be performed for 74 minutes.

(ii) Overwrite (Updating) Recording

In the 1st generation MD (MZ-1), when the REC key is pressed, empty spaces in the disc are automatically accessed and recording is started from there. When the REC key is pressed in the REC PAUSE state, over-write recording starts from that point.

In the 2nd generation MD (MZ-R2), over-write recording is even more simple;When the REC key is pressed, overwrite recording starts from the position where playing was stopped.

However in MD recorders up to the 2nd generation, if overwrite recording is performed from the middle of the disc, all tracks from the start of recording will be erased.

In MZ-R3, recording position is controlled according to the location of tracks from the start of recording, enabling tape-type overwrite recording to be performed. Therefore, even if unwanted parts on the disc are overwritten, tracks after the end of recording will not be erased like in tapes.

(Reference Information)MD recording and editing limitations

According to the MD format, more than 255 tracks (recorded areas) cannot be recorded. (The maximum number of UTOC areas that can be recorded is 255.)

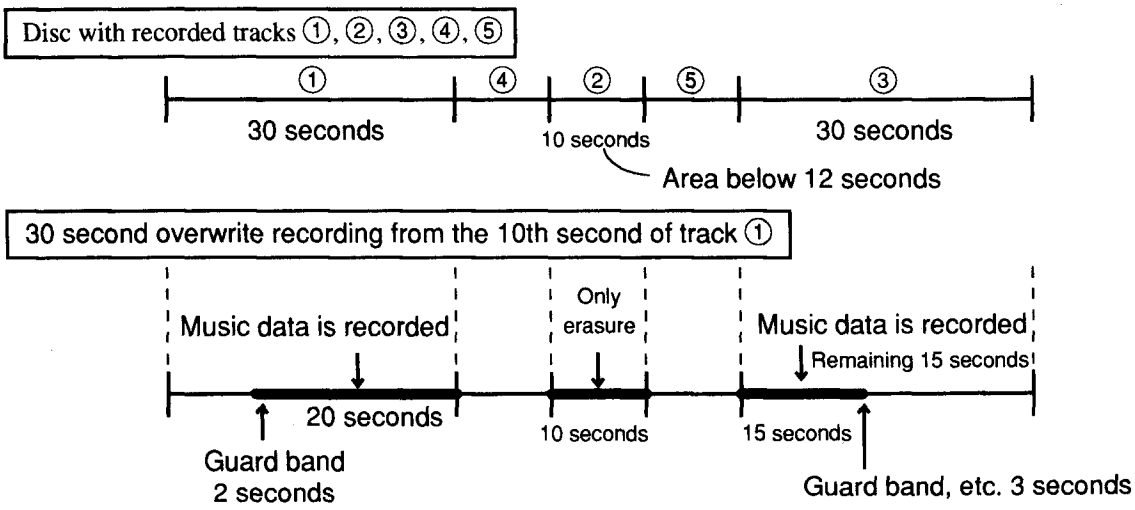
Even if overwrite recording is performed on a disc where recording areas are apart to make the track number become 1, the number of recorded area will not change. If recording and editing are repeated, the number of tracks differs greatly from the number of recorded areas. When the number of recorded areas exceeds 255, "TR FULL" will be displayed and recording will be disabled. (Refer to Fig. 1-2-3.)

(Note) Time required for erasing in overwrite recording

As guard bands (extra area to prevent accidental erasure) are set up at the beginning and end of recording during overwrite recording, the time (area) required for erasing the disc may be longer than that required for the music recording by about 2 seconds at the beginning and end, therefore a total of 4 seconds altogether. And according to the data at the start and end of recording, about 0 to 4 seconds long unrecorded areas may also be created. Therefore, the overwrite recording time and time the area is erased will not be the same.

As short recording areas (below 12 seconds) will not be recorded in the MD system, when overwrite recording is performed in such areas, music data is not recorded in these areas. These areas will only be erased.

For this reason, when overwrite recording is performed on discs with numerous short recording areas due to the repetition of recording and editing, the recording time and erasing time may differ greatly.

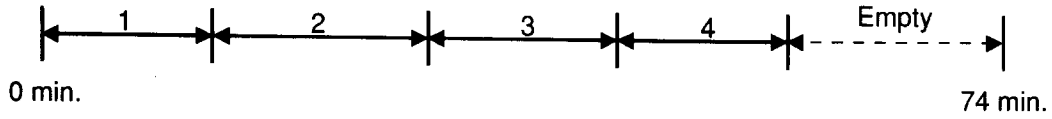


(Results)

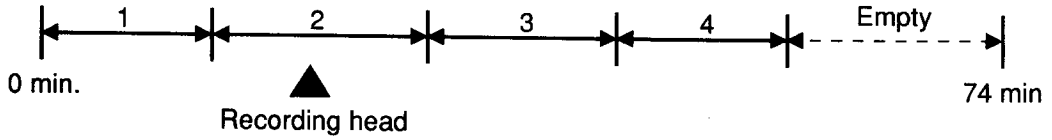
Time the music data is recorded:	30 seconds	
Time only erasure was performed:	10 seconds	
Guard band, etc.:	5 seconds	Total of 45 seconds of data is erased.

Fig. 1-2-2. Erasing Time of Overwrite Recording

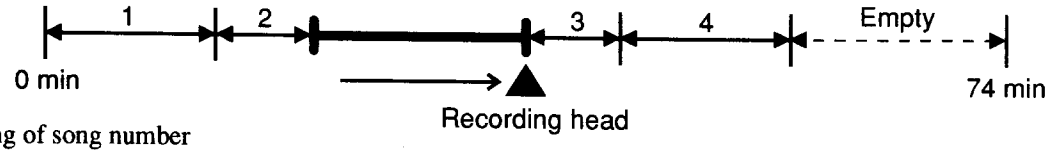
① Disc recorded with 4 songs



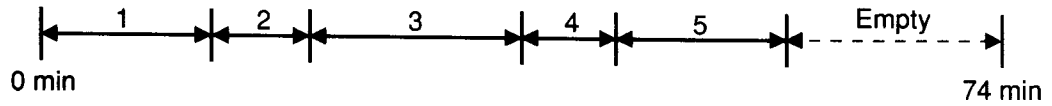
② Recording started from the middle of 2nd song



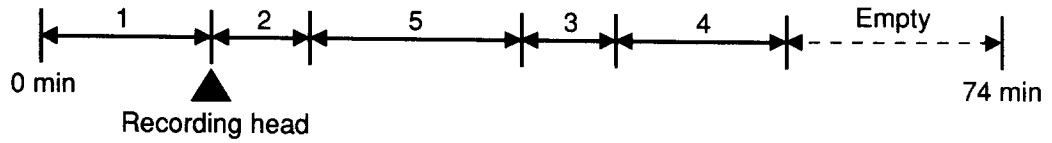
③ Recording ended from middle of 3rd song



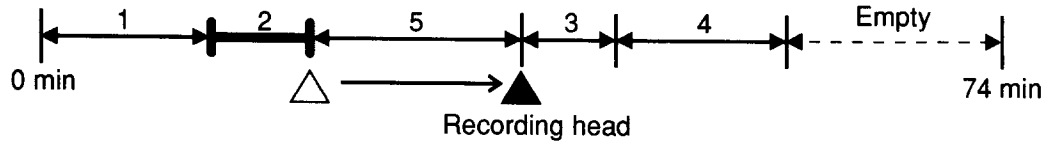
④ Resetting of song number



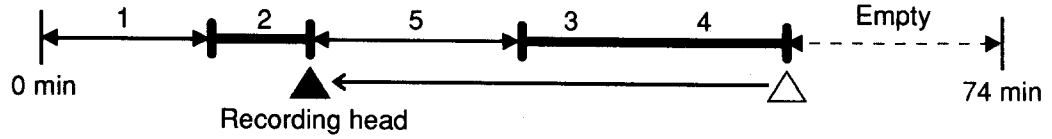
⑤ Recording started from head of 2nd song after changing song order



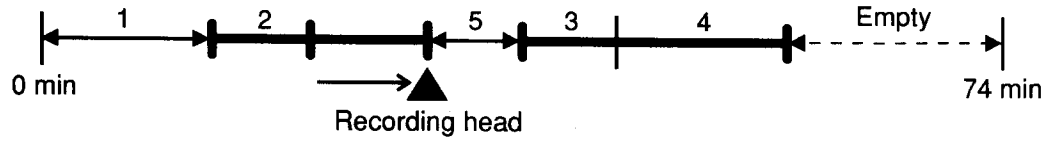
⑦ Recording continued by accessing head of 3rd song



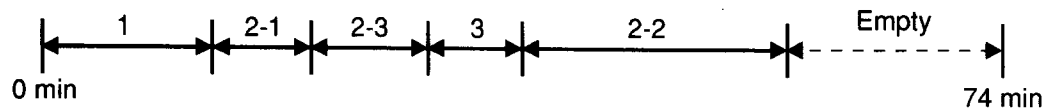
⑧ Recording continued by accessing head of 5th song



⑨ Recording ended at middle of 5th song



⑩ Resetting of song numbers



Note: The data of the 2nd song is divided into three parts on the disc.
(Played back in the order of 2-1, 2-2, and 2-3.)

Fig. 1-2-3. Overwrite (Updating) Recording

(iii) Position Pointer

A position pointer which shows at a glance the remaining space of the disc and current played back position is adopted.

This is based on the same concept as the tape window of a cassette tape and enables the state of the disc to be grasped visually during recording and editing.

The recorded area is displayed in segments and the segment blinking is the current position.

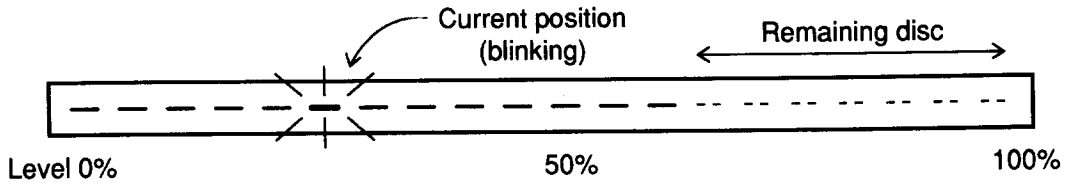


Figure 1-2-4. Position Pointer

(2) Editing Function

(i) Character Input

Characters can be input using the rotation dial. Altogether 88 types of characters can be input. They include the 26 capital and 26 small letters, 10 numerals, and 26 types of symbols (including blank). One rotation of the rotation dial makes 24 clicks. The characters complete one round in about 4 rotations. By using pressing the PLAY key, the character to be input can be selected quickly in the order of capital letter → small letter → number.

In MZ-R3, up to 200 characters can be input for one disc name and track name.

And for one MO disc, up to 1792 characters can be input. But according to the restriction of the MD format, the maximum number of characters that can be input will be less according to the length of the track name.

Characters cannot be input to BLANK disc.

(ii) Change in Song Order

The song order can be changed by pressing the TITLE/REGISTER key while pressing the PLAY key, selecting the song number to which the song is to be moved, and then pressing the TITLE/REGISTER key again.

Take note that the song number will change when the order of several songs are changed.

(3) Playback Function

(i) Monaural playback

Discs recorded in the monaural mode can be played back in the monaural mode. All the 3rd generation MD players (include home type MD players) are capable of monaural playback.

(ii) Irregular CUE/REVIEW

When the FF/REW key is pressed during playback, CUE/REVIEW operations are performed. When this key is pressed continuously, CUE/REVIEW operations will be performed at x10 speed one second later.

(Reference Information) "End" display during CUE operations

When CUE operations are performed at the end of a disc, "End" will be displayed. This is to prevent the consumption of too much time when re-accessing a disc which has ended due to excessive CUE operations during the editing of the end of that disc.

"End" display can be canceled by pressing the REW key to start REVIEW operations or pressing the STOP key. A time-out occurs in about 5 minutes, the display can be recovered using these two methods only.

(III) Fast Listening Playback...MZ-B3 Only

This function increases the playback speed to a level just before listening becomes uncomfortable without changing the tune, in order to reduce the playback time of a long recorded disc such as monaural recording, etc.

In the Fast mode, the playback speed can be selected from the x 1.6 speed (x 11/7) and x 2.2 (11/5) of the normal speed. This function can be used in both the monaural mode and stereo mode.

Quick listening playback is performed by extracting, at intervals, data stored in the shock-proof memory according to the command from the system control IC and performing ATRAC decoding. Requiring no special playback circuits, quick listening playback is executed by slightly changing the shock-proof operations according to the serial commands from the serial control IC.

(iv) Important Mark Search Function...Only MZ-B3

In MZ-B3, "important marks" can be placed at especially important points during recording.

With this function, normal track marks can be ignored and only points with the "important marks" are accessed. When the FF/REW key is pressed while pressing the VOR key during playback, the "important marks" can be searched in the Forward/reverse direction.

"Important marks" are registered as normal track marks and at the same time, the !! symbol is input at the beginning of the track name. The search for the "important marks" is accessing the start of tracks whose track names start with !!.

Therefore, if !! is input at the beginning of a normal track name in the MZ-R3 unit with the character input function, the start of the track can be taken as the important mark.

II. CIRCUIT OPERATIONS

1. Circuit Structure

(1) System Configuration

Fig. 2-1-1 shows the system configuration of the MZ-R3.

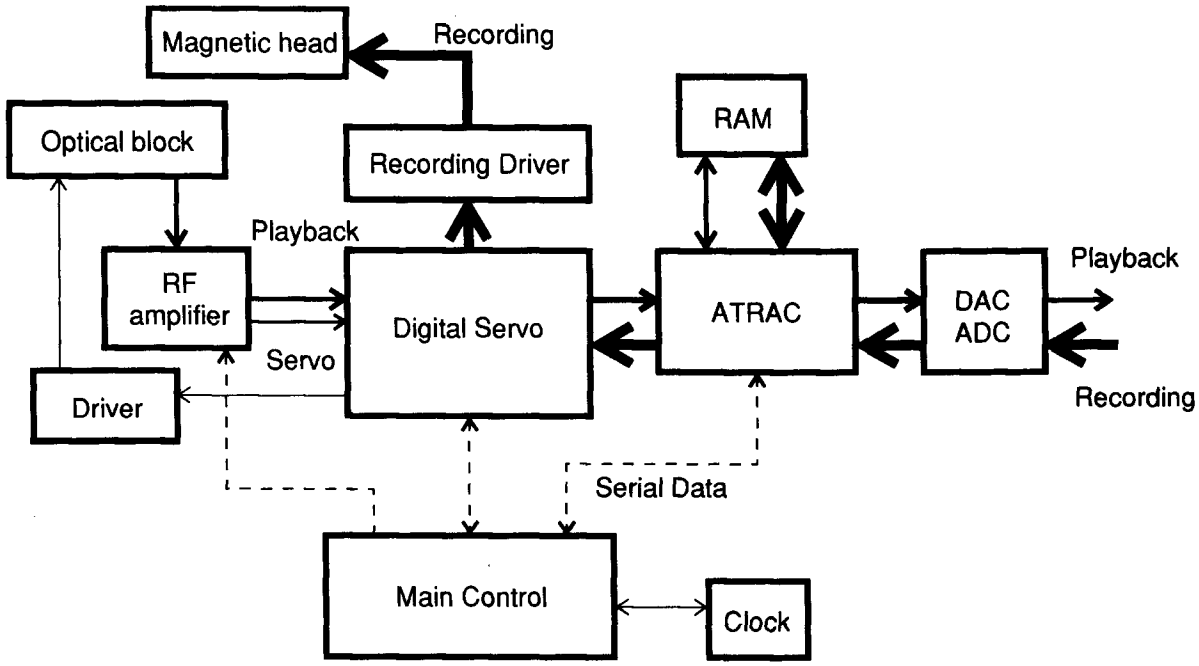


Fig. 2-1-1. MZ-R3 Circuit Configuration

(2) Main ICs

In the 3rd generation MD, all the main ICs are integrated.

Until now, address decoder, servo processing, digital signal processing (EFM, ACIRC encode and decode), and anti-shock (shock function during recording) were performed by four ICs. In the 3rd generation MD, all these processes are performed by one IC (Digital servo, CXD2535BR-1). (Refer to Fig. 2-1-2.)

Until now, shock-proof memory control and ATRAC (encode and decode) have been processed by one IC each, but in the 3rd generation MD, these are processed by one IC (ATRAC, CXD2536R).

The power supply section and display section are controlled by the system control IC. The backup function, when the power supply is not connected, is not performed by the system control IC but by the exclusive clock IC (IC804) for power conservation.

In the following chapters, the system control IC (IC801) will be referred to as "system control", the digital servo signal processing IC (IC503) as the "digital servo", and the shock-proof memory control and ATRAC processing IC (IC601) as "ATRAC".

	1st generation	2nd generation	3rd generation
Model	MZ-1 MZ-2P ZS-M1	MZ-R2 MZ-E2	MZ-R3 MZ-B3 MZ-E3
System control	Main microprocessor	Main microprocessor	Main microprocessor
Display control			
Power supply control		Sub microprocessor	
Clock backup function			Clock IC (DS1302)
RF amplifier	CXA1381R	CXA1861R	CXA1981AR
ADIP decoder	CXA1380N	CXA1380N	CXD2535BR
Servo signal processing	CXA1602R	CXA1602R	
Shock detection	PGLAD-048-ELL2000	CXD8498N	
Digital signal processing (EFM, ACIRC encoder/decoder)	CXD2525Q	CXD2525R	
Shock-proof memory controller	CXD2526Q	CXD2526AR	CXD2536R
ATRAC encoder/decoder	CXD2527R (Two used)	CXD2531AR	
Driver	MPC1718FU	MPC1718FU	MPC17A38VMEL
D/A, A/D converter	AK4501-VS	AK4502	AK4503

Table 2-1-2. Main ICs of Mini Disc

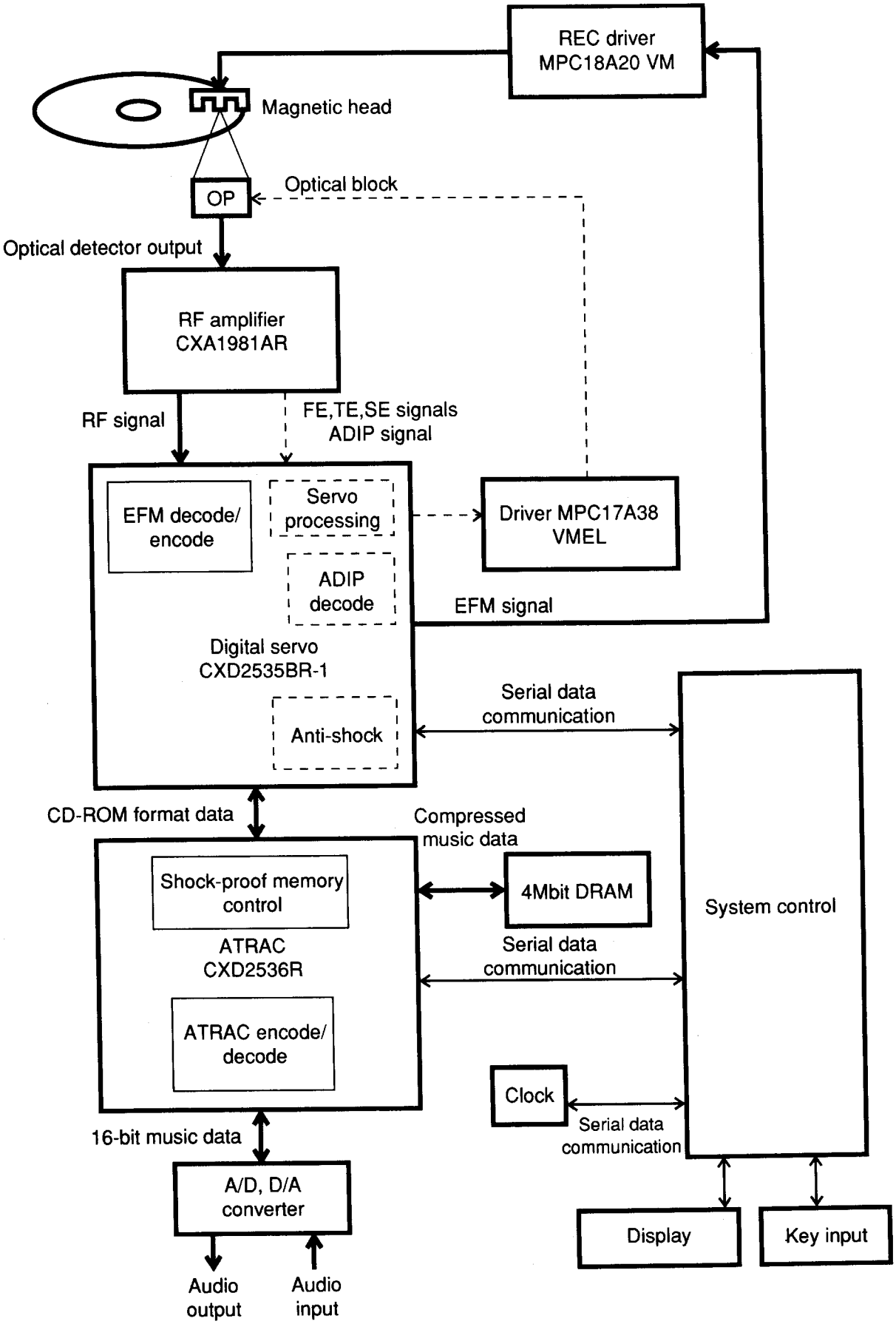


Fig. 2-1-3. Main ICs of MZ-R3

2. POWER SUPPLY CIRCUIT

(1) POWER SUPPLY

(i) Types of Power Supplies

(a) External Power Supplies

The MZ-R3 uses the following four types of power supplies.

- AC adapter (AC-E455) ..... 4.5V (Provided)
- Dry battery (AA dry battery x 2) ..... 3.0V (Optional)
- Nickel hydrogen rechargeable battery (BP-DM20) .. 2.4V (Provided)
- Lithium ion rechargeable battery (LIP-12) ..... 3.6V (Optional)

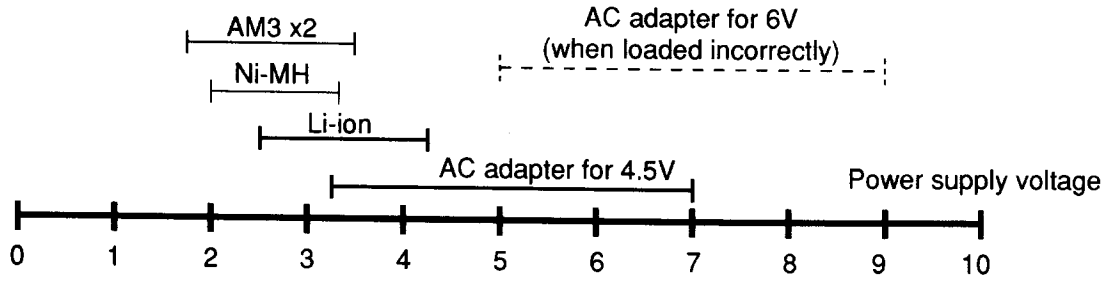


Fig. 2-2-1. Power Supply Voltage

The AC adapter and lithium ion rechargeable battery (use the battery case for LIP-12 provided) are connected to the DCIN jack. The difference between the two power supplies is detected by the battery case detection switch on the side of the DCIN jack and voltage.

The nickel hydrogen rechargeable battery and dry battery are loaded in the battery case at the bottom of the MZ-R3. The difference between these two power supplies is detected by the nickel hydrogen battery detection switch inside the battery case.

(Reference Information) Nickel Hydrogen Rechargeable Battery and Lithium Ion Rechargeable Battery

The nickel hydrogen rechargeable battery is a kind of alkaline rechargeable battery with a hydrogen occlusion alloy plate instead of the cadmium plate (negative electrode) of conventional nickel cadmium (Ni-Cd) rechargeable batteries. Its symbols are therefore Ni-MH which expresses nickel and hydrogen occlusion alloy.

Although the nickel hydrogen rechargeable battery has a higher capacity than the nickel cadmium rechargeable battery, as the two batteries have the same voltage (1.2V) between terminals, they are interchangeable.

However, in the initial stage of charging, the nickel cadmium rechargeable battery undergoes endothermic chemical reaction while the nickel hydrogen rechargeable battery undergoes exotherme reaction. Therefore when charging rapidly with a high current, rise of the battery temperature must also be taken into consideration. The charging efficiency in high temperatures and cycle life of the nickel hydrogen rechargeable battery tend to deteriorate compared to the nickel cadmium rechargeable battery.

The lithium ion rechargeable battery is a secondary battery which does not use metallic Li for its negative electrode, but substances which can absorb and discharge Li ion (Li+). It is expressed by the symbols Li-ion. The voltage between terminals when fully charged is high at about 4.2V. It is therefore not interchangeable with the nickel rechargeable battery.

The lithium ion rechargeable battery, compared to the nickel rechargeable battery, has excellent weight energy density, low self-discharge rate, and no memory effects.

(b) Backup Power Supply

The MZ-R3 incorporates a manganese lithium rechargeable battery (Mn-Li) for backing-up the clock function and resume function. The voltage of the backup rechargeable battery is 3V. When connected to an AC adapter and charged for 2 hours, it can be used for approximately 1 month.

The backup rechargeable battery is charged at voltage (2.9V) for the microcomputer when connected to external power supplies. When external power supplies are all disconnected, this rechargeable battery becomes the backup power supply of the clock IC (IC804).

In addition to the clock function, the clock IC also backs up resume data (track number, playback stop time).

(ii) Selection of power supply

(a) Priority order

When several power supplies are connected simultaneously, the one with the highest voltage will be used basically. When several of these power supplies have the same voltage, all of them will be used simultaneously.

Therefore when the fully charged lithium ion rechargeable battery (about 4.2V) and nickel hydrogen rechargeable battery (2.4V) are connected, first the lithium ion rechargeable battery will be used as the power supply. When the voltages of the two become equal, both are used.

(b) Disconnection of power supply

In conventional Discman and portable MD players, when the AC adapter is disconnected, the unit will always stop operating even if the battery is connected. This conforms to the specification which takes into account use for car battery cord. It applies to the MZ-R3 as well.

Beside the AC adapter, when a power supply is disconnected, the unit will continue operating if sufficient voltage is supplied from other power supplies.

(2) Differentiation of Power Supplies

(i) Power supply differentiation circuit

To perform charge operations and voltage drop detection, it is necessary to differentiate the type of power supply connected. Power supply is differentiated using the voltage input to the UNMNT (IC801, Pin 59), which is the system control A/D conversion terminal, and rechargeable battery detection switch (S901, S902) by dividing the plus side voltage of the power supply (UNREG).

The main detection conditions of each power supply are shown below. Under the actual differentiation conditions, even more complicated differentiation is performed to detect simultaneous connection of several power supplies, malfunction of switch, rapid voltage changes during operations, etc.

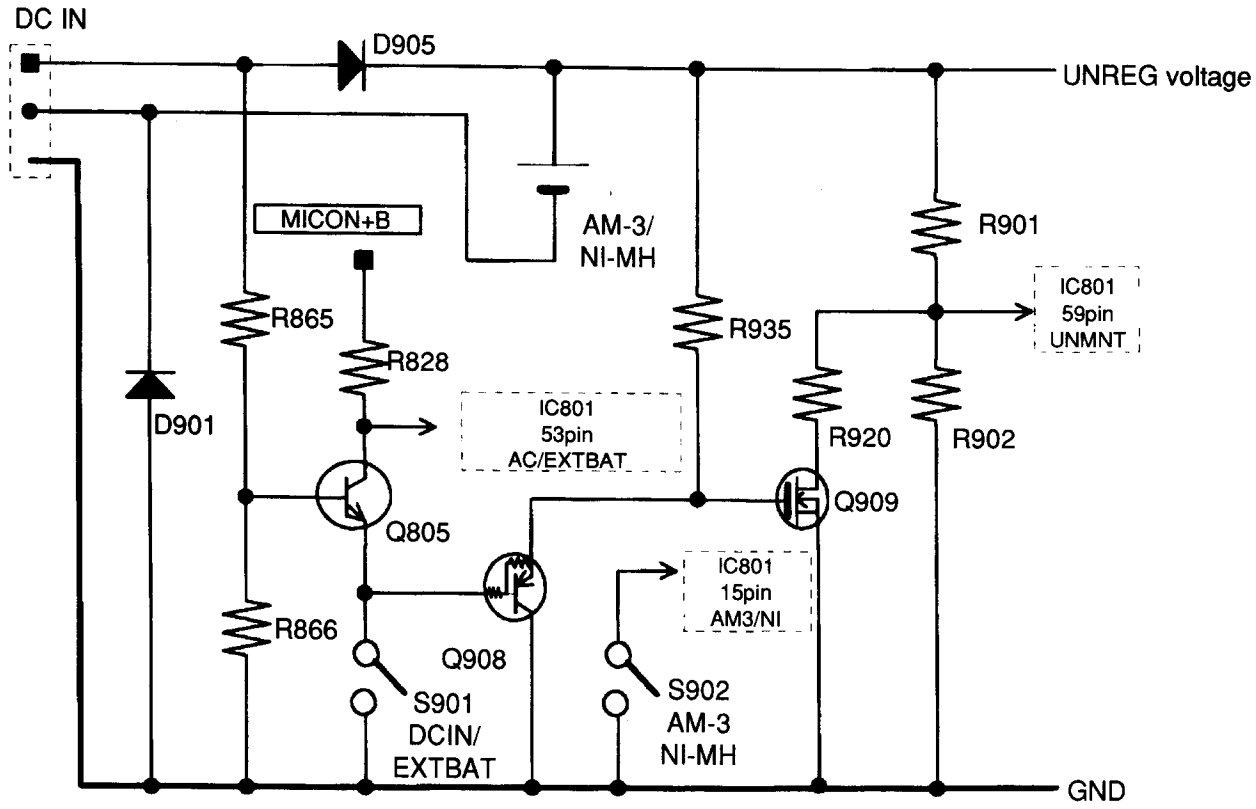


Fig. 2-2-2. Power Supply Differentiation Circuit

- AC adapter
  - Voltage is supplied to the DC IN jack.
    (Q805 turns on, IC801 Pin 53 AC/EXTBAT is H)
  - S901 (DCIN/EXTBA) is not pressed.
    (Q908 and Q909 turn on and the UNMNT voltage shifted)
  - UNREG voltage is above 3.2V.
    (The shifted voltage is detected by UNMNT Pin 59 of IC801.)
- Ni-MH rechargeable battery
  - S902 (AM-3/NIMH) is pressed....Detection of rechargeable battery
    (IC801 Pin 15 AM3/NI is L)
- Li-ION rechargeable battery
  - S901 (DCIN/EXBAT) is pressed....Battery case detection
    (As Q908 and Q909 are not turned on, the UNMNT voltage is not shifted.)
  - Voltage is supplied to DC IN...Detecion of battery
    (Q805 turned on and IC801 Pin 53 AC/EXTBAT is L)

- Dry battery
  - Voltage is not supplied to the DC IN jack.
    (IC801 Pin 53 AC/EXTBAT:H)
  - S902 (AM-3/NIMH) is not pressed.
    (IC801 Pin 15 AM3/NI:H)
  - UNREG voltage is above 1.9V.

(3) Voltage-drop detection

(i) Voltage-drop detection of batteries

(a) Detection conditions

The main conditions of voltage-drop detection of the battery are as follows.

- The terminal voltage is below 1.9V when only dry batteries are used.
- The terminal voltage is below 2.0V when only Ni-MH rechargeable batteries are used.
- The terminal voltage is below 2.6V when only Li-ion rechargeable batteries are used.

(Reference Information) Voltage between terminals of lithium ion rechargeable batteries

When the voltage between the terminals of the lithium ion rechargeable battery drops below 1V, the battery life will be affected. This is detected with 2.6V. (Voltage drops rapidly when below 2.5V.)

(b) Detection

The detection of voltage-drop is performed by the system control UNMNT terminal (IC801, Pin 59) by dividing the UNREG voltage. (Refer to Fig. 2.1.2.)

When the AC adapter is connected, Q909 is turned on, the division ratio of the UNREG voltage is changed so that it is not mixed with the battery voltage.

(Note)UNREG voltage and rechargeable battery voltage

In MZ-R3, charging current is controlled by connecting the AC adapter and the plus side of the nickel hydrogen rechargeable battery together and controlling the voltage of the minus side of the rechargeable battery.

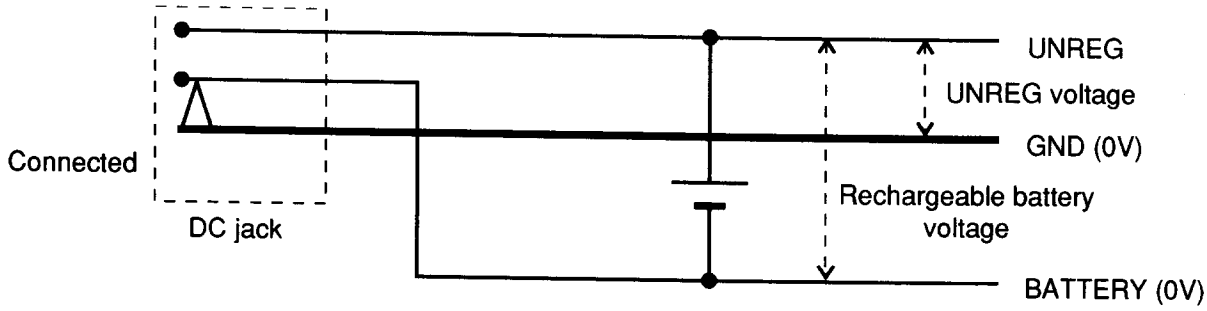
The DC jack of the MZ-R3 has three terminals. When nothing is connected to the DC jack, the minus side terminal of the rechargeable battery and GND terminal contact each other. (Refer to Fig. 2-2-3.)

The voltage between the plus side of power supplies (AC adapter, battery, etc.) and GND is the UNREG voltage. When nothing is connected to the DC jack, the UNREG voltage and rechargeable battery voltage are the same.

On the other hand, when the AC adapter or lithium ion rechargeable battery case is connected to the DC jack, the GND contact of the jack disconnects, and the minus terminal of the rechargeable battery and GND are connected by the schottky diode. As the diode decreases voltage by about 0.4V, the rechargeable battery voltage becomes greater than the UNREG voltage.

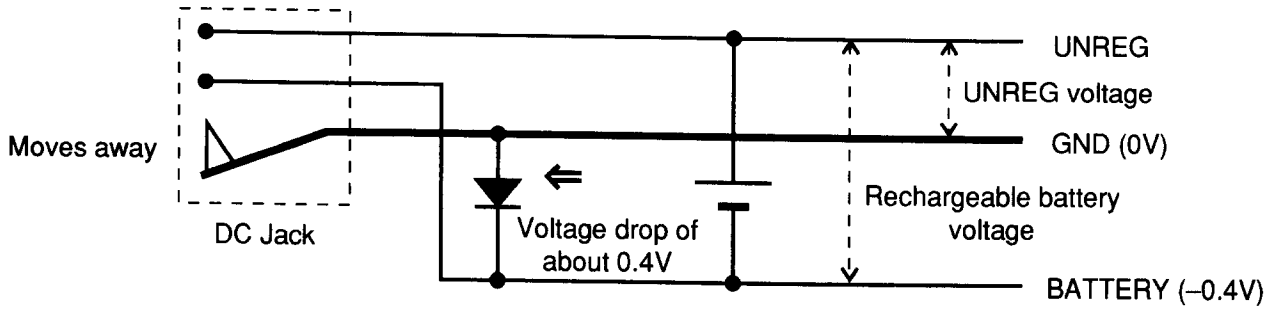
(Rechargeable battery voltage)=(UNREG voltage)+0.4V

(1) When the AC adapter and lithium ion rechargeable battery is not connected



UNREG voltage=Rechargeable battery voltage

(2) When the AC adapter and lithium ion rechargeable battery is connected



UNREG voltage < Rechargeable battery voltage

Fig. 2-2-3. UNREG Voltage and Rechargeable Battery Voltage

(c) Shift in detection voltage

When a plug is inserted in the DC jack of the MZ-R3, a difference of about 0.4V is generated between the rechargeable battery voltage and UNREG voltage. As the voltage-drop detection is performed using the UNREG voltage, if an AC adapter not connected to the outlet is connected to the jack, voltage-drop detection will be performed before the battery has been used up completely.

When it is determined as only the battery is used (UNREG voltage is below 2.5V), the output of the BATTON (IC801 Pin 31) terminal of the system control is made L. Consequently, Q906 and Q907 are turned on and the minus side of the battery (BATMNT) and GND are connected.

The rechargeable battery voltage and UNREG voltage become more or less the same due to the BATTON output. The battery power can therefore be used completely.

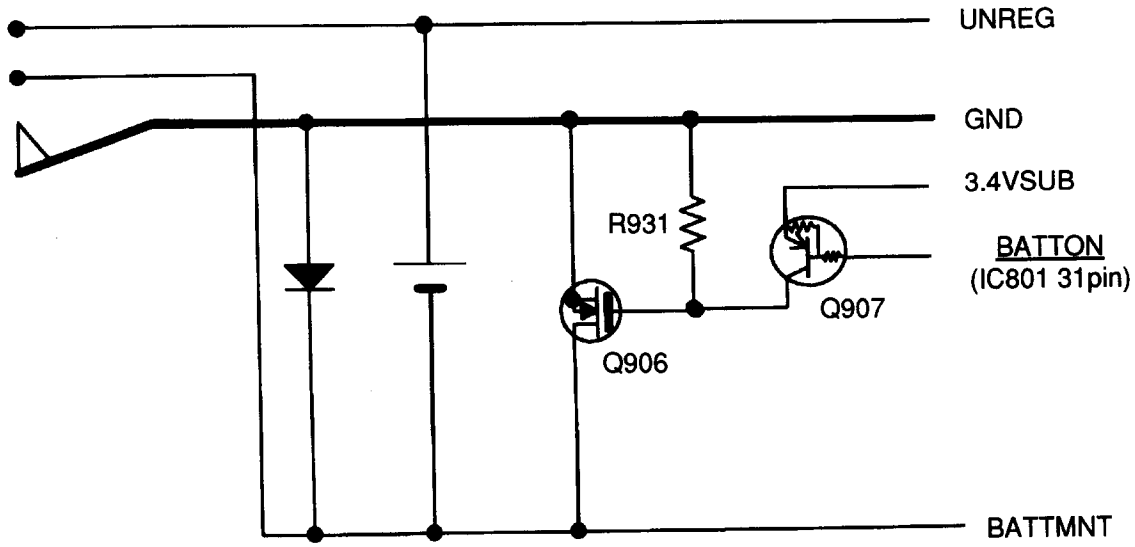


Fig. 2-2-4. Shift in Detection Voltage

(ii) Voltage-Drop Detection of DC Power

(a) Disconnection of power supply

When the AC adapter is used, one cause of drop in voltage is "disconnection of the AC adapter".

When the unit is operated by connecting several batteries and power supplies, even if one power supply is disconnected, if sufficient voltage is supplied from other power supplies, the unit will continue operating. However, when the unit is played back by connecting the AC adapter and battery, it will stop operating if the AC adapter is disconnected.

Judging from that the AC adapter is connected, it will be judged as "Disconnection of AC adapter" if the UNREG voltage becomes less than 3.2V, then it will stop operating.

(b) Connection of AC adapter for 6V

The AC adapter (AC-E455) of the MZ-R3 is for 4.5V. The diameter of the plug is the same as the AC adapter for 6V. Therefore, it may mistakenly be connected with the 6V AC adapter.

When the 6V AC adapter is connected, high input voltages (above 8V) are detected by the UNMNT terminal (IC801 Pin 59). The unit will stop operating in such cases and the "Hi DC in" error message will be displayed.

(4) Charging Circuit

(i) Rechargeable batteries

In the MZ-R3, only nickel hydrogen rechargeable batteries (BP-DM20) can be charged. Take note that it does not have a charging function for lithium ion rechargeable batteries loaded externally in the battery case. To charge these batteries, use the optional battery charger ACP-MZ60A.

(ii) Charge conditions

The following conditions are necessary to perform charging.

- Detect the connection of the AC adapter and nickel hydrogen rechargeable battery.
- STOP state of unit (Charging is not performed during operations).
- Input of the charge start key (STOP key)

If keys are input (excluding HOLD) or the AC adapter/rechargeable battery is disconnected, etc. during charging, charging is stopped.

Disconnection of the power supply (UNMNT input, detection switch) is therefore performed by system control.

(iii) Charging method

The BP-DM20 is charged by 450mA constant current. After charging, trickle charging is not performed (charging to supplement self-discharge by micro-current).

Completion of charging is detected by using the $-\Delta V$ detection method and 3-hour timer together. The $-\Delta V$ detection method detects by using the drop in voltage ($-\Delta V$) that results when the battery becomes nearly full. If $-\Delta V$ is not detected, charging is stopped 3 hours and 25 minutes from the start of charging.

If the battery voltage does not become above 2.0V within 5 minutes after the start of charging, it is determined as battery defect and charging is stopped (error message is not displayed).

Just in case detection cannot be performed using the $-\Delta V$ detection method (the battery is nearly full but the voltage has not dropped to the level for $-\Delta V$ detection to be performed), charging is also stopped when the maximum rechargeable battery voltage does not change for more than 30 minutes. (Refer to Fig. 2-2-5.)

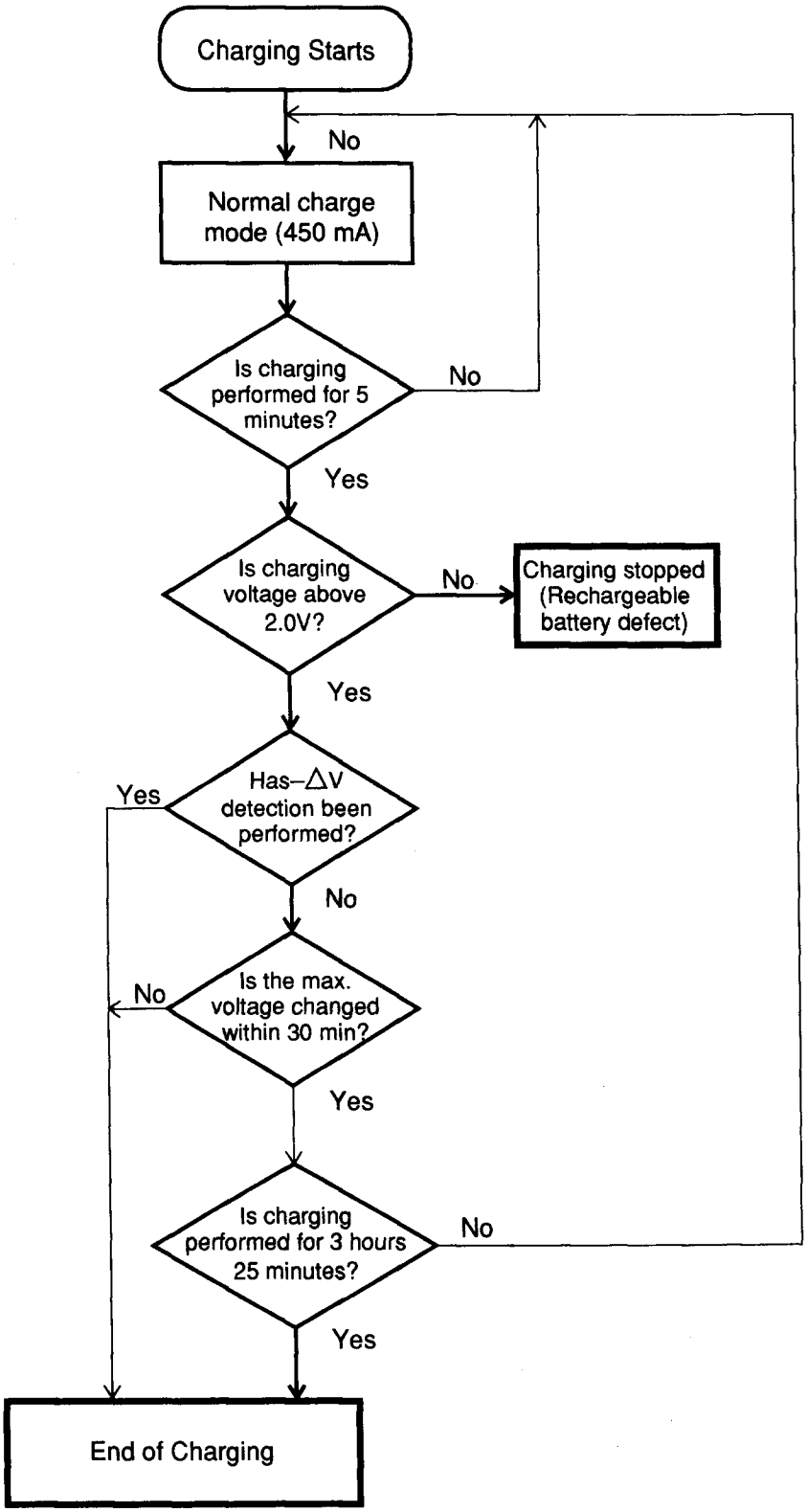


Fig. 2-2-5. Charging Flowchart

(iv) Rechargeable battery voltage detection circuit

During charging, the voltage between the terminals of the rechargeable battery is monitored and detection of rechargeable battery (disconnection detection), change in charge method, detection of completion of charge ($-\Delta V$) are performed.

In the rechargeable battery voltage detection circuit, the minus side of the rechargeable battery is connected to Pin 2 of IC901, the UNREG voltage of the plus side is resistance-divided, and input to Pin 3 of IC901. The comparison output is input to the BATTMNT terminal (Pin 60, IC801), which is the A/D conversion terminal of the system control, and the charge voltage is detected.

During charging, the CHG of the system control (Pin 100 of IC801) becomes H, Q901 and Q903 are turned ON, and the UNREG voltage is supplied to the rechargeable battery voltage detection circuit.

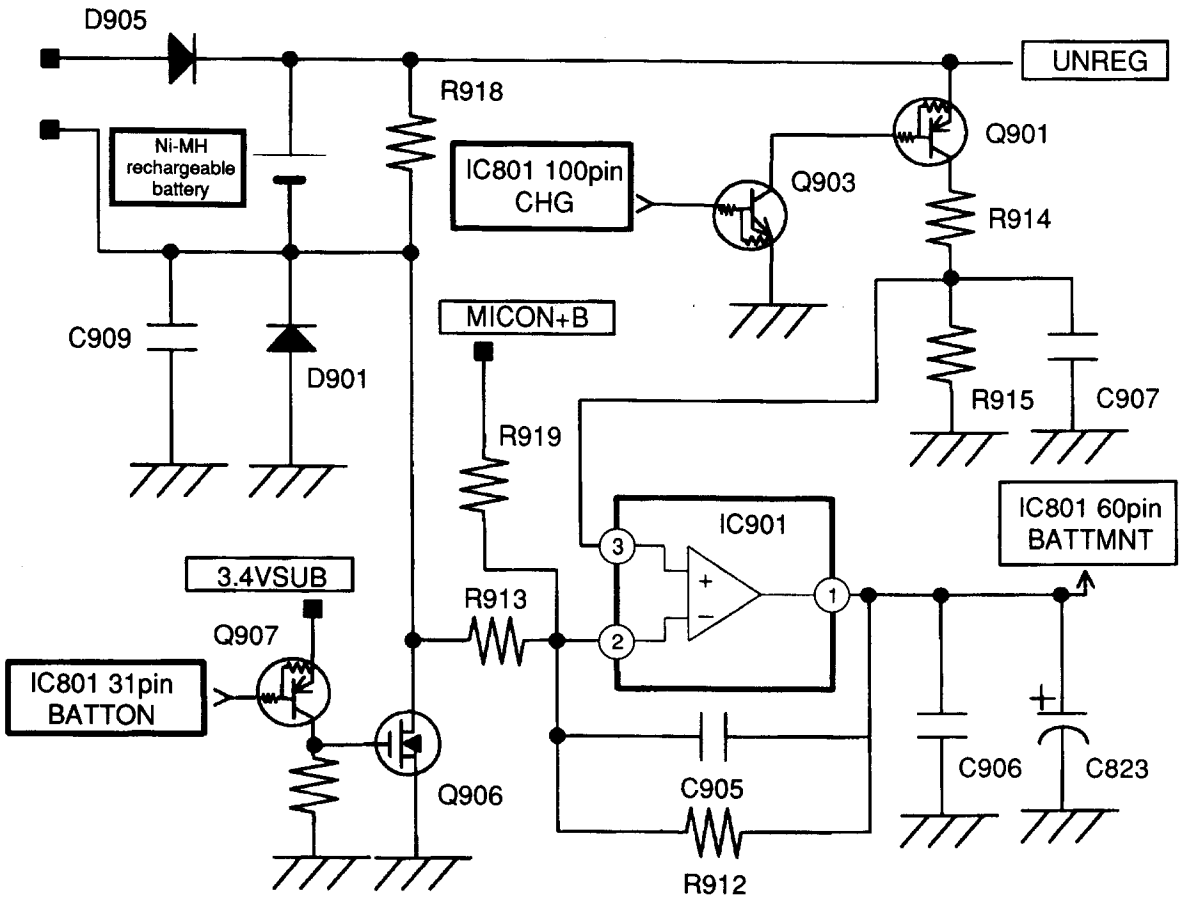


Fig. 2-2-6. Rechargeable Battery Voltage Detection Circuit

(v) Constant current charge circuit

When performing charging, the CHG terminal of the system control (IC801 Pin 100) is set to H, and Q903 and Q901 are turned on. The battery voltage is detected in the rechargeable battery voltage detection circuit to determine the charging method.

This current value is controlled by the PWM output of the CHGCONT terminal (IC801 Pin 73) of the system control.

The plus side of the rechargeable battery is connected to the plus side of the AC adapter (UNREG). The minus side is connected to the GND via Q904 and the resistor (R916, R917). The voltage value of this resistor (charging current x resistance value) is regulated to adjust the rechargeable battery current.

The voltage made by converting the PWM output from the CHGCONT terminal (IC801, Pin 73) of the system control to DC and the voltage output by the Q904 emitter are compared by IC901. The comparison output (IC901, Pin 7) is used to control Q902 and Q904 to regulate the voltage of the resistor (R916, R917).

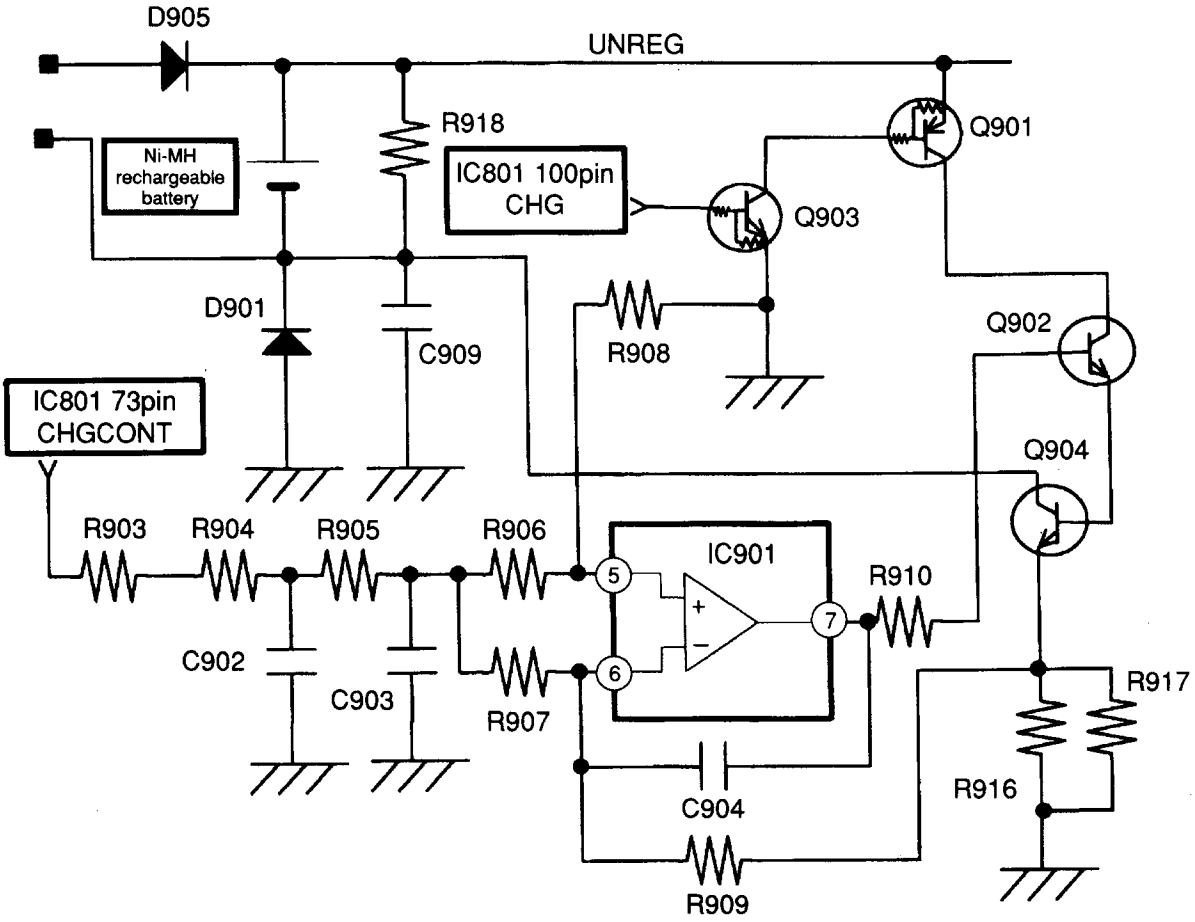


Fig. 2-2-7. Rated Current Charge Circuit

(5) Circuit Voltage

(i) Voltage of circuits

The voltage supplied to the various circuits are all made from the UNREG voltage by the regulator. The block diagram of the voltages made are shown in Fig. 2-2-8.

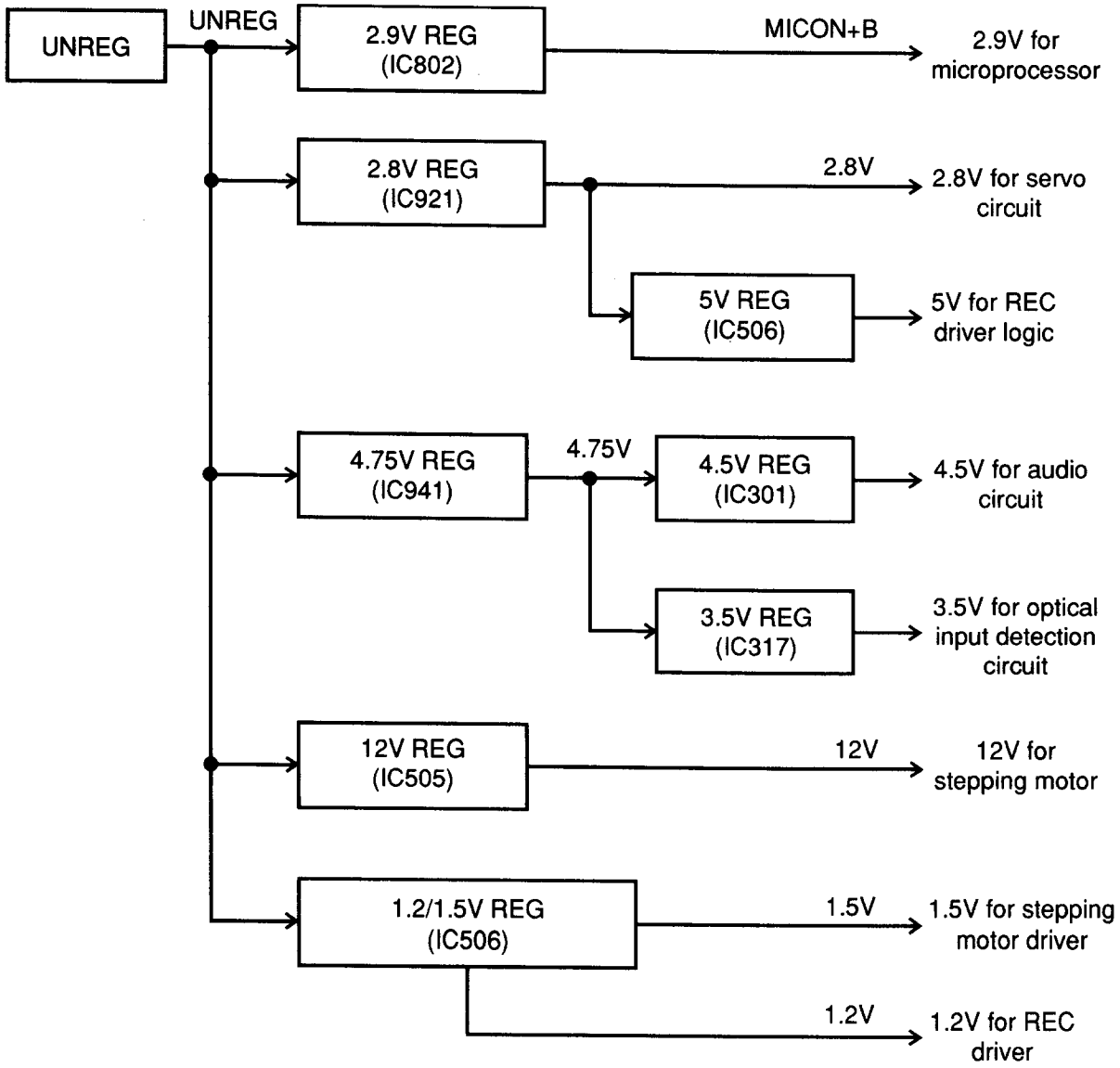


Fig. 2-2-8. Block Diagram of Circuit Voltages

(ii) Microprocessor +B voltage

When the UNREG voltage is higher than the microprocessor power supply (about 2.9V), the voltage is decreased by the series regulator inside IC802. When low, it is raised by the switching regulator composed of L801, D802, C807, and Pin 8 of IC802, and the microprocessor +B voltage is output from Pin 5 of IC802.

The microprocessor +B voltage is used as the power supply voltage of the system control (IC801), for clock backup (IC804), EEPROM (IC803), etc.

It is also used for charging the backup rechargeable battery (MNLI+) from D806.

(iii) 2.8V REG

2.8V is output from the switching of Q921 by the output of Pin 5 of IC921 and the switching regulator composed of L921, Q922, and Q923, etc.

The 2.8V output is controlled by the adjusting control RV921 which is located halfway through the feedback to Pin 1 of IC921.

The 2.8V is used as the power supply voltage of the servo circuit, optical block, etc.

(iv) 5V REG

5V is created from 2.8V for the circuits in the VG terminal (Pin 7) of the REC driver (IC506) and in the step-up converter composed of , D504, L514, C565, etc. This 5V is used as the power supply for the logic inside IC506.

(v) 4.75V REG

4.75V is output from the switching regulator composed of L941, Q942, etc. from the switching of Q941 by the output of Pin 5 of IC941.

The 4.75 output is controlled by the adjustment control RV940 which is located halfway through the feedback to Pin 1 of IC941.

The 4.75V is used for the power supply of the audio board.

(vi) 4.5V REG

The 4.5V for the audio circuit is created by the series regulator (IC301) from 4.75V.

It is used as the power supply of the AGC (IC503), control (IC315), mic amplifier (IC302), etc.

(vii) 3.5V REG

The 3.5V for the photo detector power supply of the optical IN jack (J304) is created in the series regulator (IC317) from 4.75V.

(viii) 12V REG

The 12V for the stepping motor driver (IC702) is output from the UNREG voltage by the regulator composed of the driver (IC505) and external circuit (D502, L5111).

(ix) 1.5V REG

1.5V is created by the step-down switching regulator composed of the VB terminal (Pin 25) of the REC driver (IC506) , L512, C557, etc.

The 1.5V REG is operated by the L output of the system control MODE 1 (Pin 34 of IC801).

The 1.5V created is used as the stepping motor H bridge power supply.

(x) 1.2V REG

1.2V is created in the step-down converter composed of the same circuits as the 1.5V REG-REC driver (IC506) VB terminal (Pin 25), L512, C557, etc.

The output voltage is switched to the 1.2V output by turning on Q509 with the H output of the MODE1 signal (Pin 34 of IC801) of the system control.

The 1.2V created becomes the power supply of the overwrite head driver (Q401 to Q404) on the REC board.

(Reference Information) Power supply circuit switching of the REC driver (IC506)

The REC driver (IC506) is incorporated with an internal switching power supply control circuit. It is switched using the MODE 1 and MODE 2 signals of the input signal system control (IC801).

MODE 1	MODE 2	Step-up REG	Step-down REG	Logic Section	Operating Mode
H	H	STOP	STOP	STOP	Stop, playback
L	H	Power ON	STOP	STOP	Not used
L	L	Power ON	1.5V output Power ON	STOP	Stepping motor operation
H	L	Power ON	1.2V output Power ON	Power ON	Recording

Table 2-2-1. REC Driver Mode Setting

(6) Power saving circuit

When the memory storing the data becomes full during playback operations, the MD player will set into standby during which the read disc data is not stored for a certain period of time.During recording, data of 2 seconds is compressed and intermittent recording which records in about 0.5 seconds is performed. Therefore during the 1.5 seconds during which the data is not recorded, the laser power is set to playback output and standby operations are performed.

To conserve power while batteries are used (at times other than when the AC adapter is used), the MZ-R3 turns OFF the laser output during the standby operations. Therefore, during recording and playback operations, the laser is repeatedly turned on and off so that the RF signal is output intermittently.

When the laser is off, as the servo is also off, the focus coil drive voltage is recorded in the system control (IC801) so that the servo turns on immediately after the laser turns on. The focus search is restarted using this value after the laser turns on.

(For details of the circuit, refer to the description of the servo circuit in the following chapter.)

3. SERVO CIRCUIT

(1) Laser Power Control Circuit (APC Circuit)

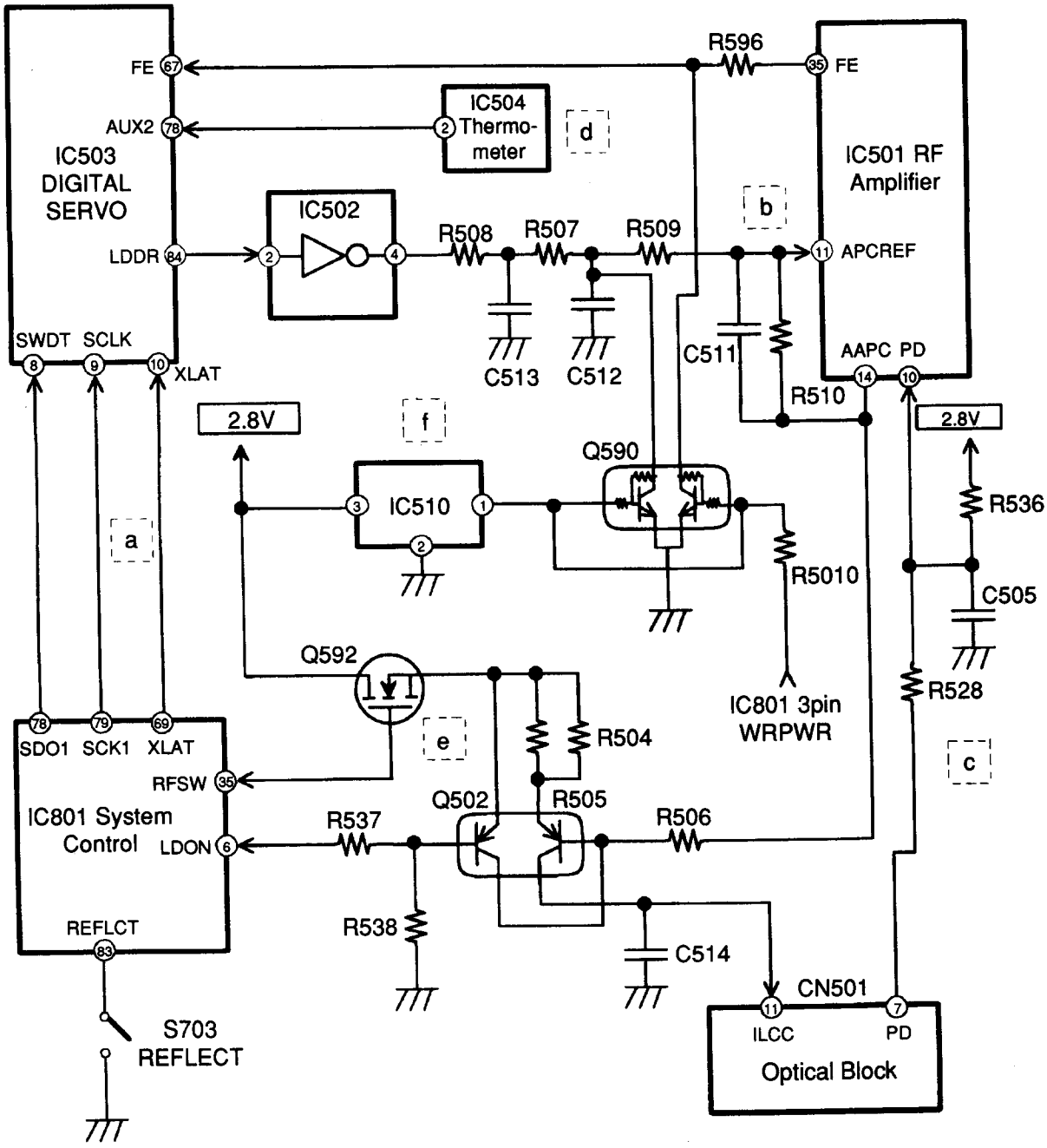


Fig. 2-3-1. Laser Output Circuit

(a) Laser Power Setting

In the MD, laser output is changed according to the type of disc used and recording/playback. The disc type (reflection rate) is checked by the detection switch using the reflectivity detection hole in the disc cartridge.

Detection switch input is detected by the REFLCT terminal (Pin 83 of IC801) of the system control.

IC801 transmits to the digital servo (IC503) the disc reflection rate and optimum recording value by the serial data from the SDO1 terminal (Pin 78). IC503 stores the data in the internal register.

IC503 controls the laser power using the PWM output of the LDDR terminal (Pin 84).

(b) Laser Current Control

The LDDR signal of the PWM output is converted to DC by the two-level low pass filter and input to the APCREF terminal (Pin 11 of IC501) of the RF amplifier. The IC502 halfway is an output inverter.

According to the APCREF input, the laser diode current flowing through Q502 is controlled by the AAPC output (Pin 14) of IC501.

When emitting the laser, the LDON of IC801 (Pin 6) is set to H.

(c) Automatic Power Control (APC)

When the laser diode is emitted by the Q502 collector output (ILCC), the monitor photo diode output (PD signal) is input to Pin 10 of IC501. The RF amplifier controls the AAPC output according to this monitor output so that the laser power becomes constant.

(d) Temperature Compensation During Recording

During recording, the Pin 2 output of IC504 which changes the output voltage according to the temperature is read by the A/D conversion terminal (AUX2 Pin 78 of IC503), and during recording, the laser power value (LDDR PWM output of Pin 84 of IC503) is compensated. These temperature compensation operations are performed inside IC503.

(e) Laser Output ON/OFF

While batteries are used in the MZ-R3 (at times other than when the AC adapter is connected) and during recording/playback data reading standby, the laser output is turned off to conserve power.

During data reading standby, the RFSW terminal (Pin 35 of IC801) is made L, Q592 is turned off, and the voltage supply to the optical block and RF amplifier is stopped.

(f) Rush Voltage Prevention

When the voltage during start-up of the unit is unstable, the optical block laser diode will become damaged if a high voltage is supplied to it.

To prevent this, the optical block voltage is detected by IC510. When the voltage for the optical block (2.8V) is above 3V, Pin 1 of IC510 outputs H.

Q590 is turned on by this H output and the laser drive output of the digital servo IC (Pin 84 of IC503, LDDR) is muted.

(2) Automatic Adjustment of Servo Circuit

The MZ-R3 has automatic adjustment functions for its servo circuit. Therefore, gain, EF balance, and focus bias are automatically adjusted by the unit's test mode program.

These automatic functions are performed only at shipment and are used as data, which is memorized in the EEPROM (IC803), thereafter. (Some of these adjustments are performed each time the power is turned on.)

The automatic adjustment functions can be executed again in the test mode.

- Automatic adjustment at shipment (Thereafter EEPROM recorded data is used)
  - E-F balance adjustment (CD/CDL/MO read/MO write)
  - Focus bias correction (CD/CDL/MO)
  - Focus/tracking gain adjustment (CD/CDL/MO)
- Automatic function performed each time disc is replaced
  - ABCD level adjustment (CD/CDL/MO read/MO write)
- Automatic adjustment performed each time power supply is connected
  - Offset cancel of VC, FE, and ABCD signals

(a) E-F balance adjustment

The E-F balance automatic adjustment is performed by serial data communication between the digital servo (IC503), system control (IC801), and RF amplifier (IC501).

(Refer to Fig. 2-3-2.)

By switching the internal switch, the E-F balance adjustment resistance of IC501 can be changed. This switch is switched by the serial data from IC801.

According to the set value of the serial data from IC801, the TE signal which had been E-F balance-adjusted is output to IC503. IC503 compares the SE signal (TE signal converted to DC value) with VC, and the difference is transmitted to IC801. IC801, according to result, changes the traverse adjusted value of IC501.

This is repeated until the difference between the SE signal converted to DC and VC is minimum. IC801 records the traverse adjusted value as the optimum value in the EEPROM (IC803). IC803 is also called the NV (non-volatile) RAM. IC801 reads and writes data by serial data communication (SDIO2 Pin 17 of IC801).

IC801 reads the recorded adjusted data while the unit is operating, transmits it to the digital servo (IC503) and RF amplifier (IC501) and sets it.

(b) ABCD level adjustment

The ABCD output level is A/D converted by the digital servo (IC503) and transmitted to the system control (IC801) in serial data form.

Like the E=F balance adjustment, IC801 switches the internal gain switch in IC501 by the serial data, adjusts the ABCD level, and sets the optimum value.

(c) Gain adjustment

Gain adjustment is performed inside the digital servo IC.

The FE, TE signals input from the RF amplifier are 8-bit A/D converted by the 88.2 kHz sampling frequency and the SE signal by the 345 Hz sampling frequency. After gain adjustment and phase compensation is performed in digital processing, error signals are PWM output using the D/A converter inside IC503.

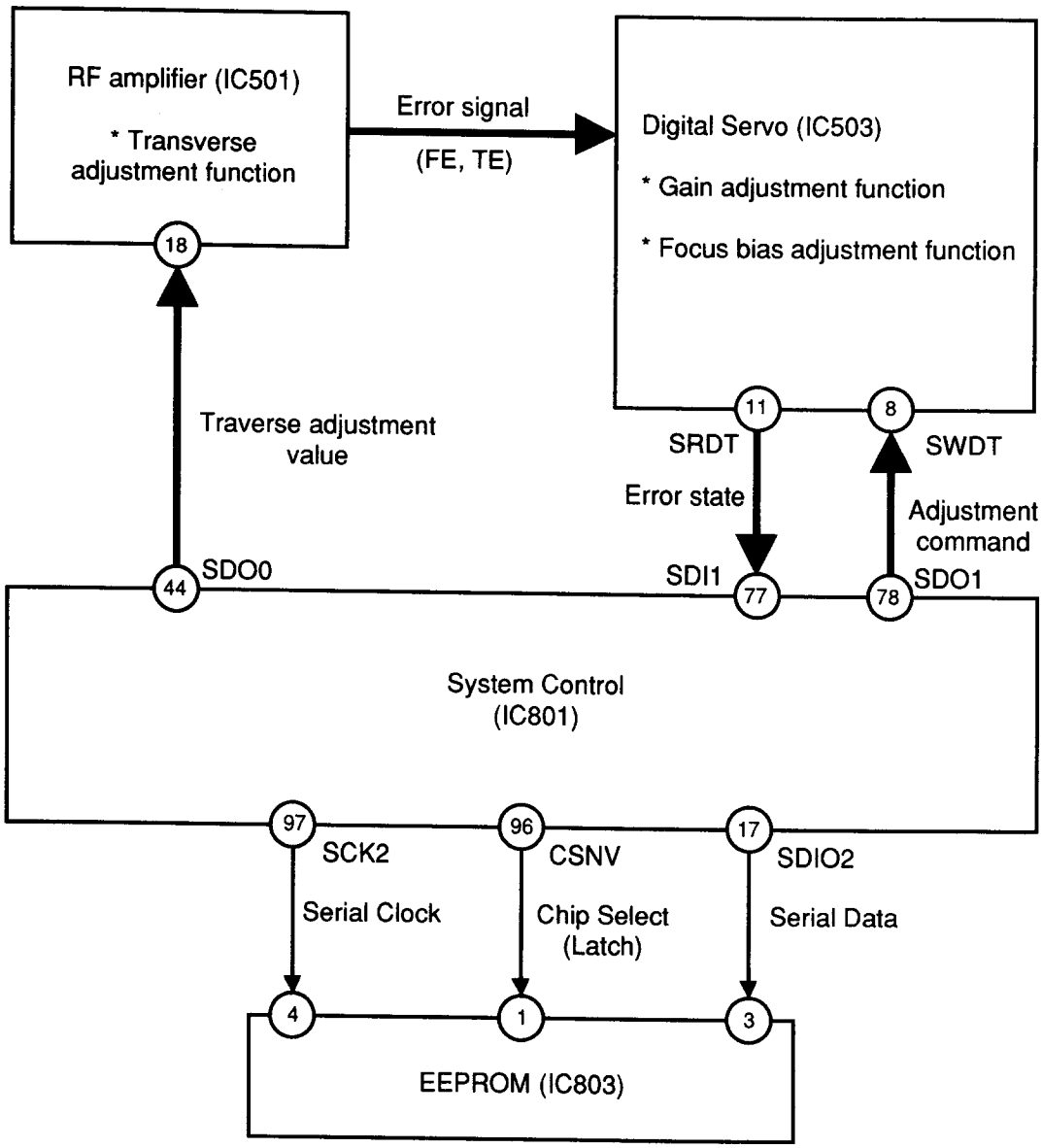


Fig. 2-3-2. Automatic Adjustment Circuit

(3) Focus Servo Circuit

(a) Focus search operations

To turn on the focus servo, focus search operations are started. First, the auto sequencer inside the digital servo (IC503) is started up by the serial command from the system control (IC801).

The auto sequencer executes the focus search operation sequence set by the digital servo, and raises and lowers the objective lens by driving the driver using the PWM output. At this time, when focus is turned on (FOK becomes H, zero-cross-point of the S-curve signal), the focus servo is turned on automatically.

(b) Intermittent operations (Recording/playback)

In the MZ-R3, the laser is turned off during recording/playback data reading standby when batteries are used. (Servo operation is off) When the laser is turned on again, the servo circuit is started up. but at this time, servo is not turned on by normal focus search operations.

To turn on the focus servo immediately after the laser turns on, the focus coil drive voltage is buffered in IC508 and the input voltage is memorized by the IC801 (47) FDMON terminal of the A/D conversion terminal. After the laser turns on, focus search is performed according to this value.

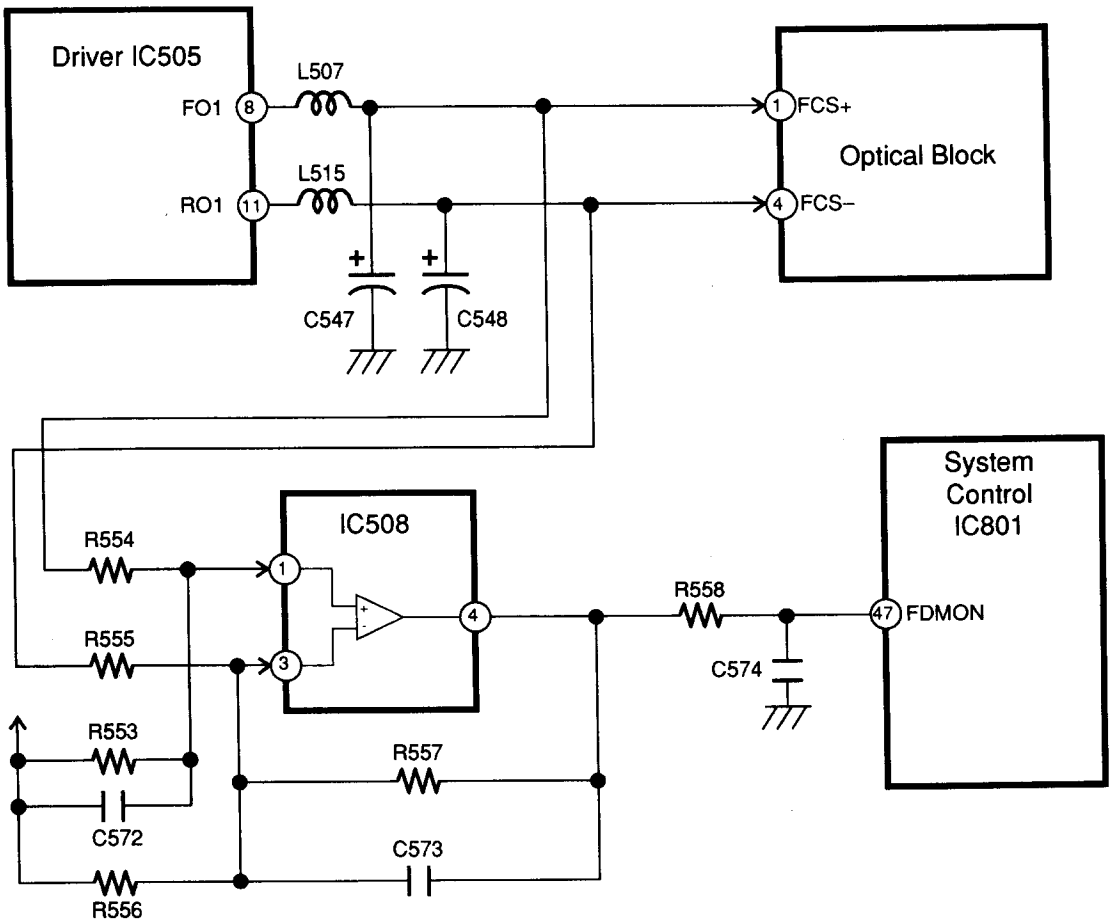


Fig. 2-3-3. Simple Focus On Circuit

(4) Tracking Sled Spindle Servo Circuit

According to the auto sequencer incorporated in IC503, the servo is turned on in the following order.

Focus → Tracking and sled → Spindle

(a) Tracking servo

According to the TE signal (Pin 77 of IC503) from the RF amplifier, the driver (IC505) drives the tracking coil using the PWM output (Pin 87/89 of IC503).

(b) Sled servo

According to the SE signal (Pin 76 of IC503) from the RF amplifier, the driver (IC505) drives the sled motor using the PWM output (Pin 91/92 of IC503).

(c) Spindle Servo

During pit area playback, the RF signal output from the RF amplifier (Pin 41 of IC501) is EFM decoded inside the digital servo (IC503) and the sync signal for the spindle servo is extracted.

During groove area playback, the ADFG signal output from the RF amplifier (Pin 33 of IC501) is ADIP decoded inside the digital servo and the sync signal for the spindle servo is extracted. The ADFG signal is an approximately 22 kHz signal output (A+D)-(B+C) of the photo detector.

The driver (IC505) controls the spindle motor driver (IC701) according to the output from the SPFD/SPRD terminal (Pin 94/93 of IC503) and drives the spindle motor. The BRK input (Pin 22) of IC701 serves as the input of the absolute value for the motor rotation direction while the VS input (Pin 16) serves as that of the motor rotation speed.

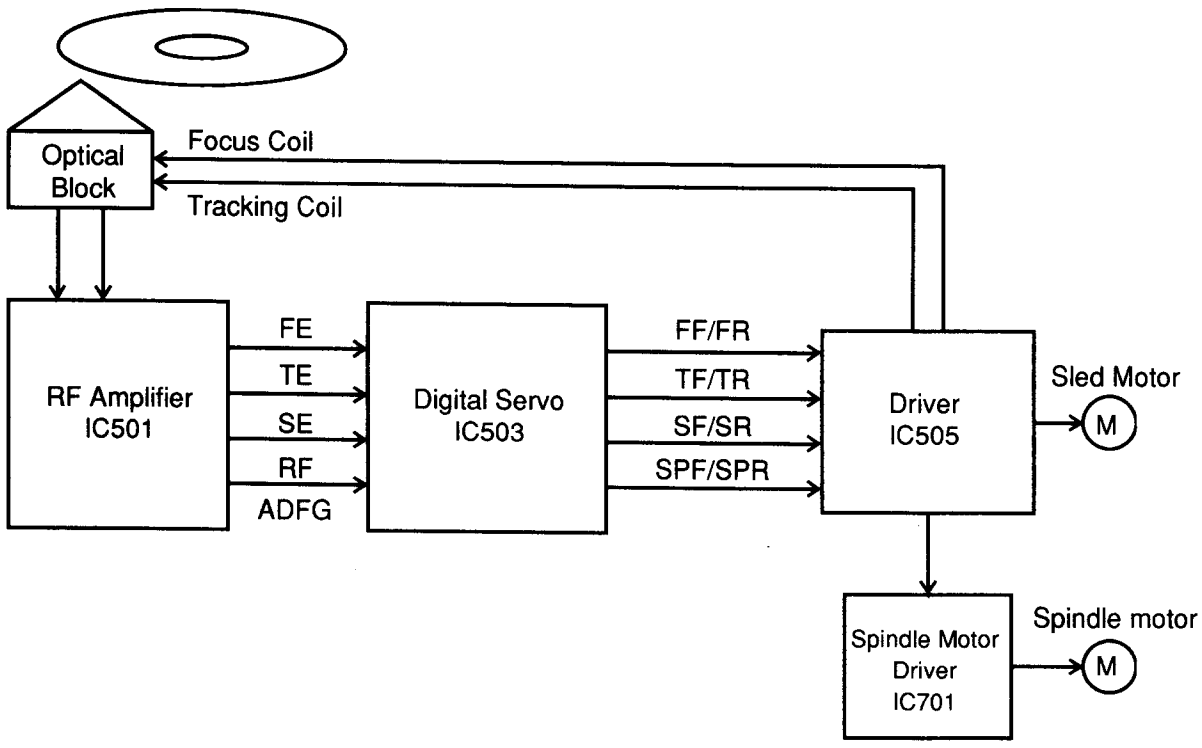


Fig. 2-3-4. Tracking, Sled, Spindle Servo Circuit

4. Signal Circuits

(1) Playback Operations

(i) Detection of playback state

(a) Upper panel locking

When the power supply is connected to the unit, the locking of the upper panel is checked with the OPEN switch (S817). If it is not locked, nothing is displayed when keys are input.

(Take note that this is easily mistaken for power fault.)

(b) Presence/absence of disc

Next, the presence of the disc is checked with the MEDIA switch (S704). When determined as no disc, "NO DISC" is displayed even if the PLAY key is pressed.

(c) Reflectivity of disc

When the OPEN switch is pressed, if the MEDIA switch is pressed, the reflectivity of the disc is detected by the REFLECT switch (S703). The unit sets the laser power according to the reflection rate, the laser emits, and focus search operations are performed. (At the same time, the spindle motor performs kick operations.) At this time, if the focus servo does not turn on, "DISC ERROR" is displayed.

(d) Moving of optical block

When the focus servo turns on, the pit/groove determination of the optical block position is performed inside the digital servo according to the reflected light from the disc. According to this result, the servo mode is set, the disc address is read, and the pit area in the inner circumference of the disc is accessed.

Therefore, when the optical block is at the groove area, first, up to the innermost groove area is accessed. Next, pit/groove determination is performed while the optical block is moved further inside, and when it is determined as the pit area, the servo mode is changed to the setting for pit so that the lead-in area information (TOC) can be read.

During the start-up of the unit, the INLIMIT switch (S705) which performs innermost area detection is not used. This switch is used for resetting only when the optical block position cannot be determined due to shocks occurring during disc playback.

(ii) Reading of TOC information

For the optical disc (CD), the lead-in area TOC data is read, while for the magneto-optical disc (MO), the read-in area PTOC data and recordable area UTOC data is read.

For the MO disc, after the lead-in area PTOC data in the pit area is read, only the focus servo is turned on to rotate the sled motor for a certain period of time to move the optical block to the groove area. (During sled operations, the groove area playback data is set.)

The TOC data track information is stored in the shock-proof operation RAM (IC602). During playback, the playback circuit is switched according to the information for each track (emphasis ON/OFF, monaural/stereo switching).

(iii) Other operations

(a) Recording circuit power OFF

To conserve the power of the unit, voltage supply to the recording audio circuit and optical IN jack is stopped by the outputs of the OUTSEL terminal (Pin 92) and OPTCTL terminal (Pin 94) of the system control (IC801).

(b) Monaural playback

The monaural-recorded track is determined according to the track information and the ATRAC (IC601) is switched to the monaural mode using the serial data from the system control (IC801). In the monaural mode, the audio signal of one channel is input to the left and right channels and output to the D/A converter.

As the amount of data decoded is 1/2 during normal playback, the playback pause time of intermittent reading increases.

(2) Playback Circuits

(i) RF amplifier (IC501, CXA1981)

The RF signal is generated according to the disc playback position (pit/groove) from the I and J detectors of the optical block. The switching of the pit/groove signals is performed using the serial data input to the SWDT terminal (Pin 18 of IC510) from the system control (IC801).

(Refer to Fig. 2-4-1.)

(ii) Digital servo (IC503, CXD2535BR-1)

The EFM signal is generated from the RF signal input to the digital servo (IC503), EFM decoding, and ACIRC decoding (deinterleave) are performed, and the CD-ROM format data is output from the DTO terminal (Pin 30) to the ATRAC (IC601).

Based on the X601 (45.158 MHz, 1024 fs) connected to Pins 36 and 37 of ATRAC (IC601), the clock for data output is frequency divided by 1/2 by IC601, and from the 512 fs (22.579 MHz) input to the XTAI terminal (Pin 35 of IC503) of the digital servo, the BCK terminal (Pin 32) outputs 2.8 MHz and the LRCK terminal (Pin 33) outputs 44.1 kHz.

(iii) ATRAC (IC601, CXD2536R)

The CD-ROM format data input to the DATA terminal (Pin 93) is decoded and only the music data is stored in the 4M bit DRAM (IC602). The data uses 9 address lines and 4 data lines.

IC601 has a shock-proof memory processing function and ATRAC decode function. It expands the compressed data to 16-bit music data, synchronizes with LRCK and BCK, and outputs to the D/A converter (IC304).

(iv) D/A converter (IC304, AK4503)

The music data (SDTI), BCK, and LRCK from the ATRAC IC (IC601) and the 256 fs (11.2895 MHz) from the digital servo (IC503) are input and analog output.

The system control (IC801) switches the deemphasis using the output of the DEEMP terminal (Pin 89) according to the track emphasis information. (L:Emphasis ON)

Using the PDDA signal (Pin 90 of IC801) from the system control, the D/A converter circuit inside the D/A converter (IC304) is started up. To conserve power at this time, the power of the A/D converter inside the IC304 is turned down using the PDAD signal (Pin 91).

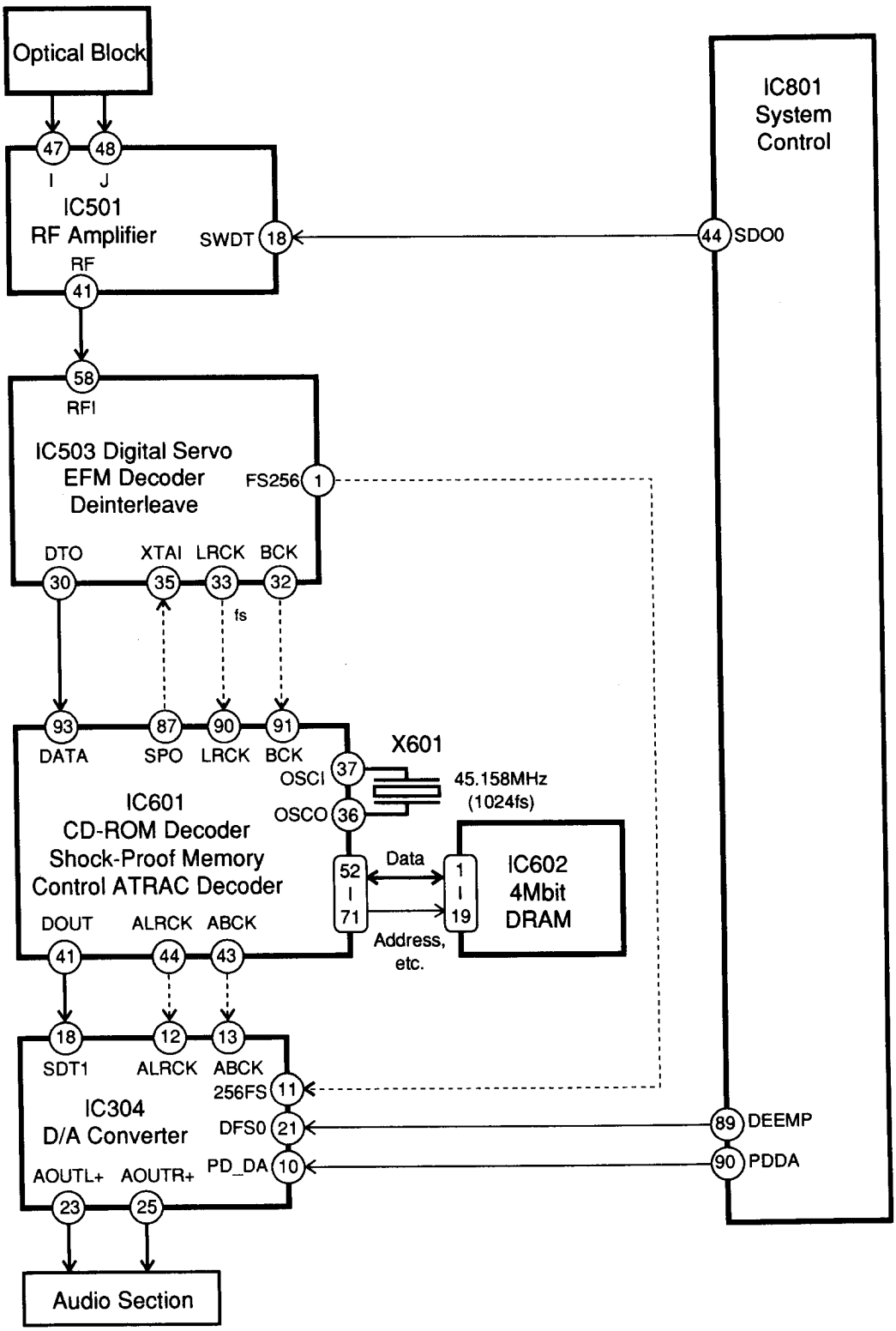


Fig. 2-4-1. Playback Circuit

(v) Headphone Control (IC352)

The serial data (SDIO2 Pin 17 of IC801) of the system control is input to the headphone control DIN terminal (Pin 4 of IC352) to adjust the headphone output control. The CSHP terminal (Pin 95 of IC801) output is a chip select signal. It turns on Q306 when H and mutes the serial data and clock input (SCK 2).

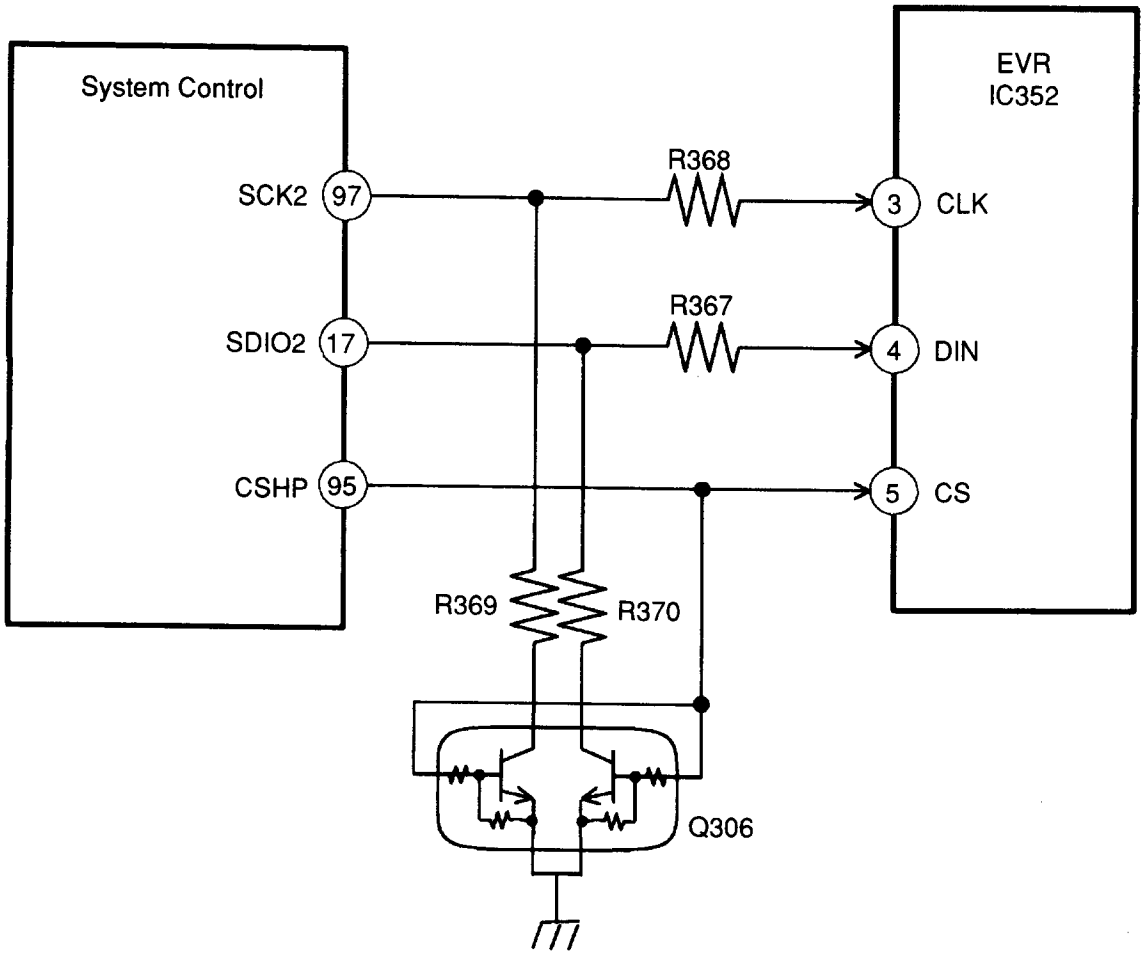


Fig. 2-4-2. EVR Control Circuit

(vi) Beep Sound Generation Circuit

The beep sound is generated by turning on and off Q320, Q313, and Q314 according to the output of the BEEP terminal (Pin 81 of IC801) of the system control.

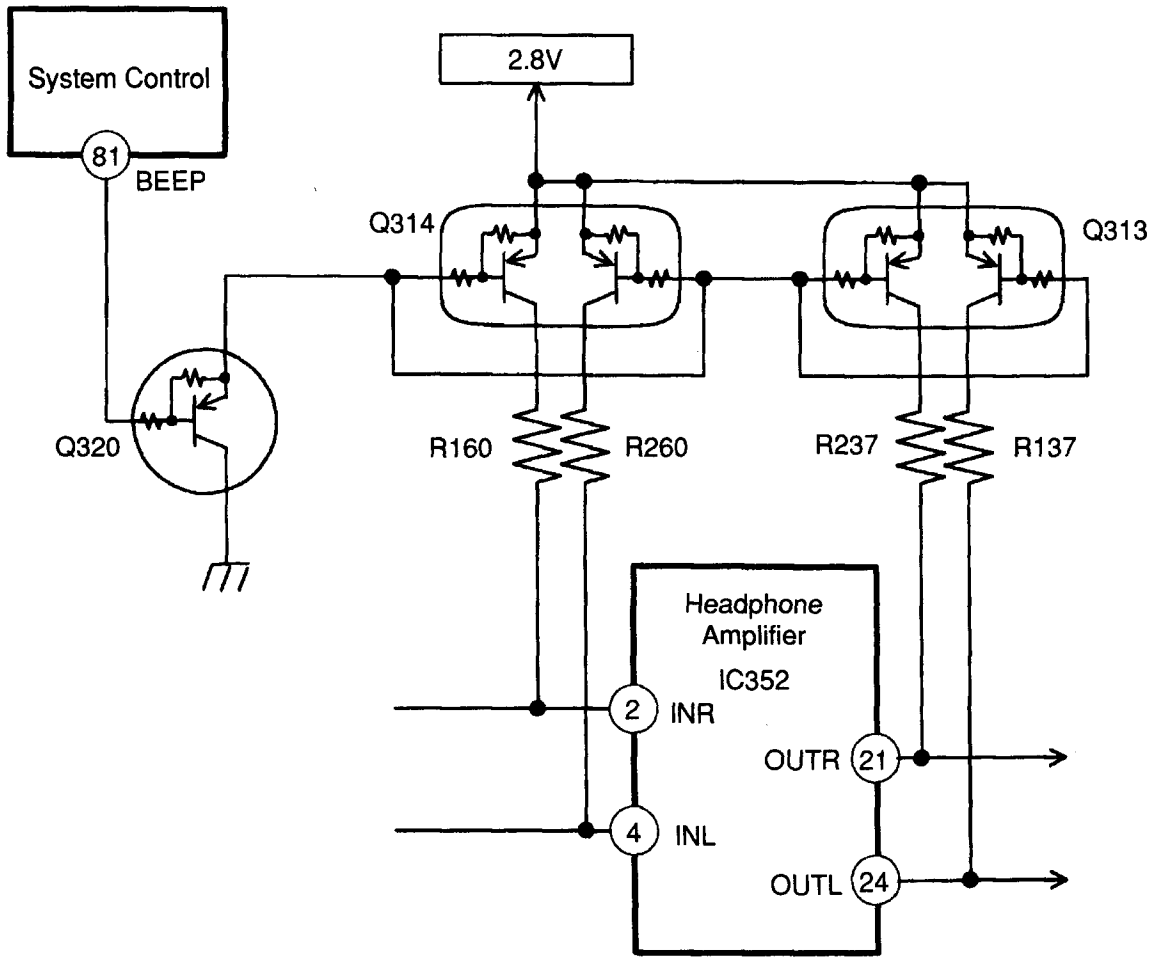


Fig. 2-4-3. Beep Sound Generation Circuit

(vii) Analog Mute Circuit

The output of the AMUTE terminal (Pin 93 of IC801) of the system control is input to the MUTE terminal (Pin 30 of IC308) of the headphone amplifier and the headphone output is muted.

The AMUTE signal turns on Q318, Q309, Q102, and Q202, and mutes the line OUT output.

(3) Recording Operations

(i) Setting of recording state

(a) Detection of REC-proof state

When a disc is loaded into the unit, the rec-proof state is checked using the PROTECT switch (S702). When the rec-proof knob (white) is slid and the hole is opened, recording is not set even when the REC key is pressed and "PROTECTED" is displayed.

When the REC key is pressed when a playback only disc is loaded, "PB DISC" is displayed by the reflectivity detection of the disc.

(b) Recording mode

In the recording mode of MZ-R3, the mode is switched to monaural or stereo. When recorded in the monaural mode, recording of double the time of the stereo mode can be performed. (120 minutes for a 60 minute disc, 148 minutes for a 74 minute disc).

The recording mode is set by the input of the MODE key during REC PAUSE. When the monaural mode is set, Pins 1 and 2 of IC301 are short-circuited by the MON/ST terminal (Pin 29 of IC801) of the system control, and the Lch and Rch of the stereo input are mixed.

The ATRAC encode processing is switched to the monaural mode by the serial data output from the system control to the ATRAC (IC601).

(c) Determination of input

There are three input sources-digital (optical) IN, line IN, and mic IN. The line IN jack is used for digital IN as well, and the type of input source used is detected by the GND part of the inserted stereo mini-plug.

Input is determined by mic jack detection (Pin 68 of IC801 MICDET), optical jack detection (Pin 67 OPTDET), and optical + line jack detection (Pin 66, JACKDET). The detection conditions are as follow.

	MICDET (68pin)	OPTDET (67pin)	JACKDET (66pin)
Connection of mic IN jack	L	— —	— —
Connection of optical IN jack	— —	H	L
Connection of line In jack	— —	L	L
No connection	H	H	H

Table 2-4-1. Input Determination

When the input sources are connected simultaneously, the priority given is optical IN, mic In, and then line IN. Therefore if the optical cable is connected, mic input cannot be recorded.

When the input source is the optical IN, the digital input is determined by the ATRAC processing IC (IC601) using the serial data from the system control IC (IC801) and encode processing is performed.

When the input source is mic IN, Q315 is turned on and power is supplied to the mic amplifier (IC302). Secondly, Q393 is also turned off, the INSEL terminal of the AGC amplifier (Pin 18 of IC303) becomes H, and the analog input switches from line to mic.

(ii) Switching during recording

(a) Recording laser power

The mini disc performs intermittent recording of music data in clusters. Therefore during recording operations with no shock, the music data is recorded for 0.5 seconds only and the next 1.5 seconds is set to the playback pause state. (When batteries are used, during the no recording 1.5 seconds, the laser is turned off.)

For this reason, the recording/playback laser output value recorded in the internal register of IC503 is switched by the signal to the digital servo (IC503) from the WRPWR terminal (Pin 3 of IC801) of the system control. (H:recording power. L:playback power)

(b) Shock detection

When subjected to shock during recording and the servo is turned off, the recorded area will be erased. For this reason, shock is determined when track jumps occurs during recording.

The shock detection during recording is performed inside the digital servo (IC503). When shock is detected, the recording power is switched to the playback power, and the SHOCK signal is sent to the system control (IC801).

The TCOUNT terminal (Pin 76 of IC801) of the system control is used also as the terminal for detecting the SHOCK signal detection pin from the digital servo. As the TCOUNT signal is used only during accessing, and the SHOCK signal is used only during high laser power in recording, they are not output at the same time.

The two signals are switched by switching the internal switch of the IC507 by the WRPWR terminal (Pin 3 of IC801) of the system control which outputs the high laser power state during recording.

When the SHOCK signal is detected by IC801, playback laser power setting and re-accessing of the recording position are performed.

When IC801 switches the settings, the internal shock detection circuit of IC503 is reset by the output of the SHCKEN terminal (Pin 99 of IC801) and the next shock is detected.

(c) Digital IN PLL

When the optical cable is connected, the input is determined as digital IN by the detection of the jack part, and the system control (IC801) starts up the digital IN PLL of the digital servo (IC503) using the serial data.

The digital IN PLL extracts the sync signal from the digital IN signal and locks. This is performed inside the digital servo (IC503) using the serial data (input switching) from the system control (IC801).

When there is no optical signal, or of the signal cannot be read properly, as the digital IN PLL is not locked, "NO SIGNAL" will be displayed.

If the input signal is read properly, and digital copy is prohibited by SCMS, "NO COPY" is displayed.

(iii) Editing Function

When editing operations such as, changing the track-marking position or inputting the name of the track, are performed after recording, first the UTOC data stored in the RAM is rewritten. Then the UTOC data of the RAM is overwritten in the disc when the STOP key is pressed. During overwriting, "Toc Edit" is displayed blinking.

Therefore, if the power supply is disconnected without pressing the STOP key after editing operations, the disc data will not be rewritten.

(4) Recording Circuit

(i) Mic/Line input

The audio signal input is input from the mic amplifier (IC302), control (IC315), AGC amplifier (IC303), differential amplifier (IC101) on the audio board to the A/D converter (IC304) on the main board via the flexible board.

(Refer to Fig. 2-3-3.)

IC304 starts up the A/D converter circuit by the PDAD signal (Pin 91 of IC801) from the system control. To conserve power at this time, the power of the D/A converter circuit is decreased by the PDDA signal (Pin 92) output.

The analog signal input is A/D converted in 16-bit by IC304, synchronized with the ABCK signal and ALRCK signal, and output to ATRAC (IC601) from the SDTO terminal (Pin 14).

(ii) Digital input (IC503)

The optical input digital signal is input to the digital servo (IC503) and decoded in the digital audio interface format.

From the category code of the input signal and copy prohibit code, according to SCMS, the able/disable of the digital copy is determined. When copy is prohibited, "NO COPY" is displayed.

When copy is permitted, 16-bit music data is output to the ATRAC encoder (IC601) from the DIDT terminal (Pin 28 of IC503).

(iii) ATRAC Encode Shock-Proof Memory Operations (IC601)

(a) ATRAC encode

The digital (DIDT signal)/analog (DIN signal) input is selected according to the serial data from the system control.

The selected 16-bit music data is ATRAC encoded and compressed by about 1/5.

(b) Shock-proof operations

The compressed music data is stored in the 4M-bit DRAM, the data is summarized in clusters and output to the DTI terminal (Pin 29 of IC503) of the digital servo from the DATA terminal (Pin 93 of IC601).

(iv) EFM encode interleave (IC503)

The data input in clusters is subject to the interleave (ACIRC) and EFM encoded in the digital servo (IC503). The EFM signal is synchronized with the disc signal in the encode PLL composed of the IC503 internal phase comparator, LPF (IC603, etc.), VCO (D601, etc.), and output from the EFMO terminal (Pin 45) to the recording driver (IC506).

(v) Recording driver (IC506) and magnetic head

The EFM signal input to the EFM terminal (Pin 14) of the recording driver (IC506) drives the overwrite head driver (Q401, Q402, Q403, Q404) of the REC board by the outputs of the HA terminal (Pin 11) and HB terminal (Pin 10), and outputs the recording magnetic field data from the magnetic head to the disc.

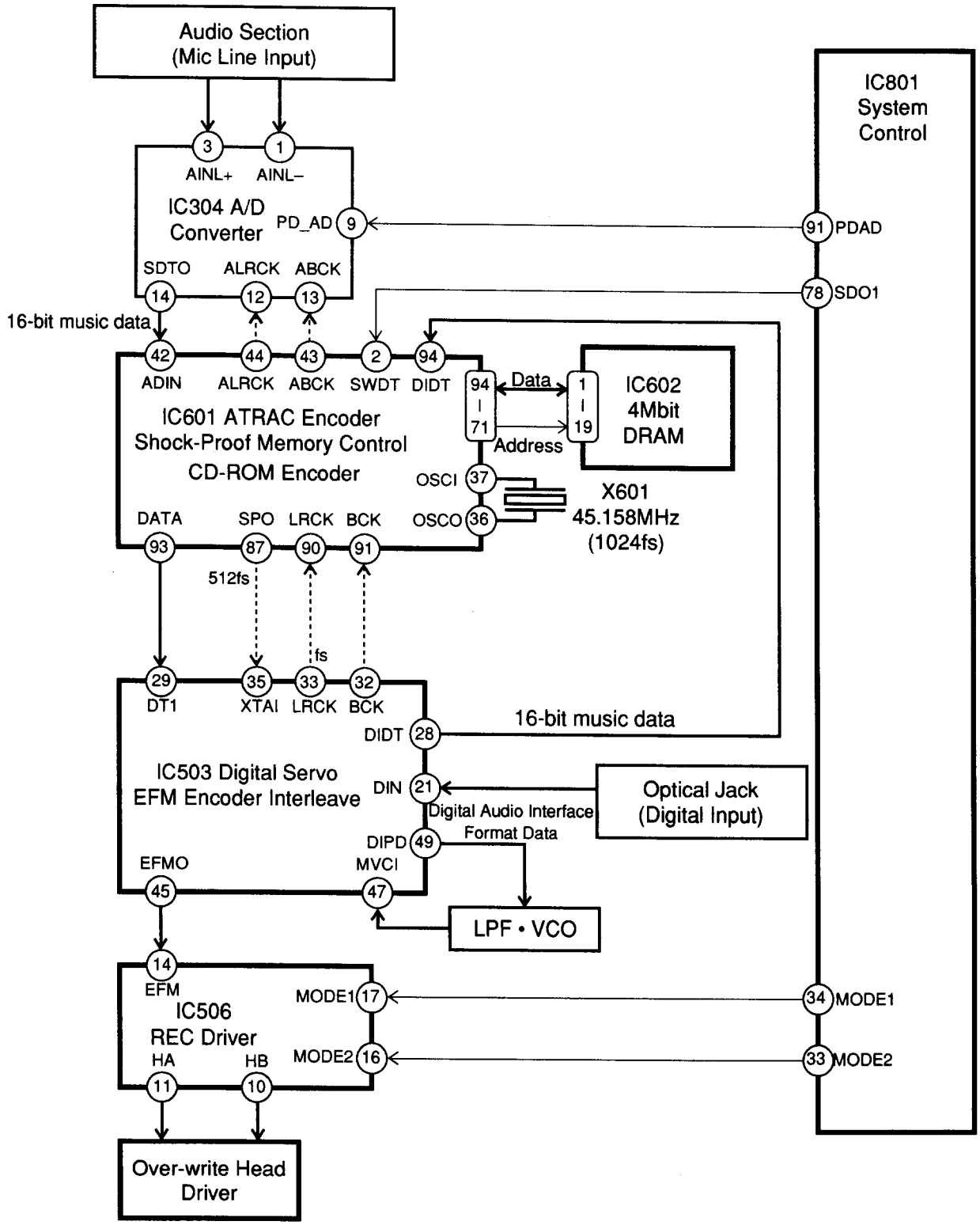


Fig. 2-4-4. Recording Circuit

5. Mechanism Operations Control Circuit

(1) Mechanism mode

The MZ-R3 uses the same mechanism as the 2nd generation MZ-R2. There are three mechanism modes. They are as follows.

- Eject mode

  Mode in the stop state in which disc can be ejected. The top cover opens when the OPEN key is slidden.

  When the PLAY key is pressed, the playback mode is set. When the REC key is pressed, the recording mode is set via the playback mode.

  It is equivalent to mode 210 (STEPPER display) in the mechanism test mode.

- Playback mode

  Mode to playback the disc. The disc holder will be locked and the disc cannot be ejected. (The OPEN key is ignored.)

  When the STOP key is pressed, the EJECT mode is set again.

  It is equivalent to mode 211 (Can't Open display) in the mechanism test mode.

- Recording mode

  Mode for recording the disc. Like the playback mode, the top cover will be locked and the magnetic head will descend on to the disc.

  It is equivalent to mode 212 (R_HEAD ON display) in the mechanism test mode.

(2) Stepping motor

The mechanism mode is changed by the rotation of the stepping motor. The slider of the mechanism chassis is moved by the rotation of the motor. Connection release of the EJECT key, holder lock, and descent of the magnetic head are performed.

When the stepping motor is rotated in the normal direction for a certain period of time from the stop state (eject mode), the playback mode is set. Furthermore, when the motor is rotated in the constant period of time, the recording mode is set.

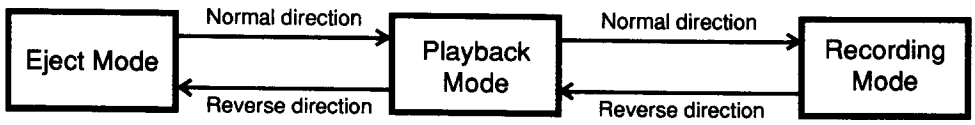


Fig. 2-5-1. Mechanism Mode Change

(Note)Disc jamming due to power supply failure

When the power supply is cut off when the mechanism mode is in the playback or in the recording mode, the holder of the disc is locked, and as the EJECT key will not work, the disc cannot be removed. In this case, connect the power supply again so the disc is ejected.

If the disc cannot be ejected due to power supply faults or mechanism faults, open the main board and rotate the gear of the stepping motor with your finger and set the EJECT mode so that the disc can be removed.

At this time, make sure not to scratch the gear by using the driver for rotating the gear.

(3) Mechanism mode change

The detection of the mechanism mode is performed by the INITIAL switch (S704) on the CLV board. The switch is pressed when the EJECT mode is set. The switch input is detected by the INTSW terminal (Pin 64 of IC801) of the system control.

When the power supply is connected to the unit, INITIAL switch detection is performed. When the EJECT mode is not set, rotate the stepping motor in the reverse direction to set the EJECT mode.

Next, when the disc is loaded in the unit, the TOC information is read and the disc information is displayed on the display. The mode is still EJECT mode at this time.

When playback is started by pressing the PLAY key, the rotation of the stepping motor is sounded and the mode is changed to the playback mode. But it will be some time after the PLAY key is pressed that the mode changes to the playback mode completely.

When the REC key is pressed in the STOP state, the stepping motor rotates more than the playback mode and the recording mode in which the magnetic head descends is set. Although the mini disc performs intermittent recording, the magnetic head always contacts the disc during the REC state.

(4) Stepping Motor Control Circuit

Q701 on the CLV board is turned on by the L output of the MODE 1 signal (Pin 34 of IC801) from the system control. 2.8V is supplied to the stepping motor driver (IC702) and the IC702 internal logic switch (Q702) is started up.

The MODE 1 signal turns off Q509, changes the voltage value input to the INM terminal (Pin 1) of the REC driver (IC506), and the 1.5/1.2V regulator outputs 1.5V by the switching output of IC506. (1.2V is output during recording head driving.)

The 2.8V input to the VC terminal (Pin 5) of IC702 is the power of the IC702 logic section. The 1.5V input to the VM1 and VM2 terminals (Pins 2 and 11) is the H bridge power of the output. The 12V input to the VG terminal (Pin 12) is the power of the internal level shift section.

The rotation of the stepping motor (M903) is controlled by the ST1SOU/ST2SOU output (Pins 71 and 72 of IC801) of the system control.

The ST1SOU/ST2SOU outputs are input to the IN1A and IN2A terminals of the stepping motor driver (IC702). The ST1SOU/ST2SOU inverted signals are input to the IN1B and IN2B terminals in Q702.

The phase of the ST1SOU and ST2SOU outputs is shifted by 45° with the DUTY 50% pulse signal. The two OUT1A and OUT2A terminal outputs of IC702 are also phase-shifted by 45° to drive the stepping motor.

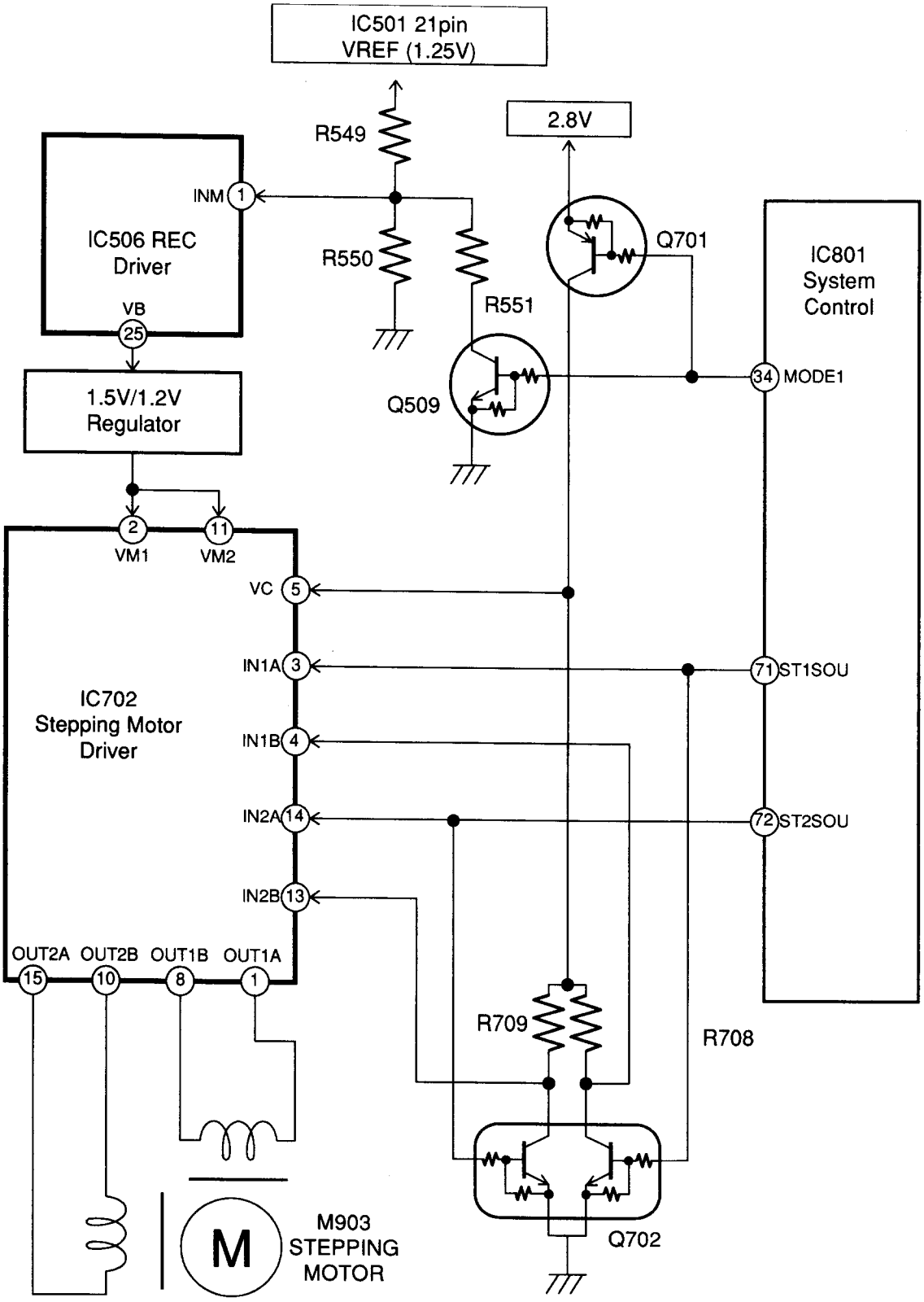


Fig. 2-5-2. Stepping Motor Control Circuit

IN1A/IN1B (IN2A/IN2B)	OUT1A (OUT2A)	OUT1B (OUT2B)
L/L	L	L
L/H	H	L
H/L	L	H
H/H	Z	Z

Table 2-5-1. Stepping Motor Driver Input/Output

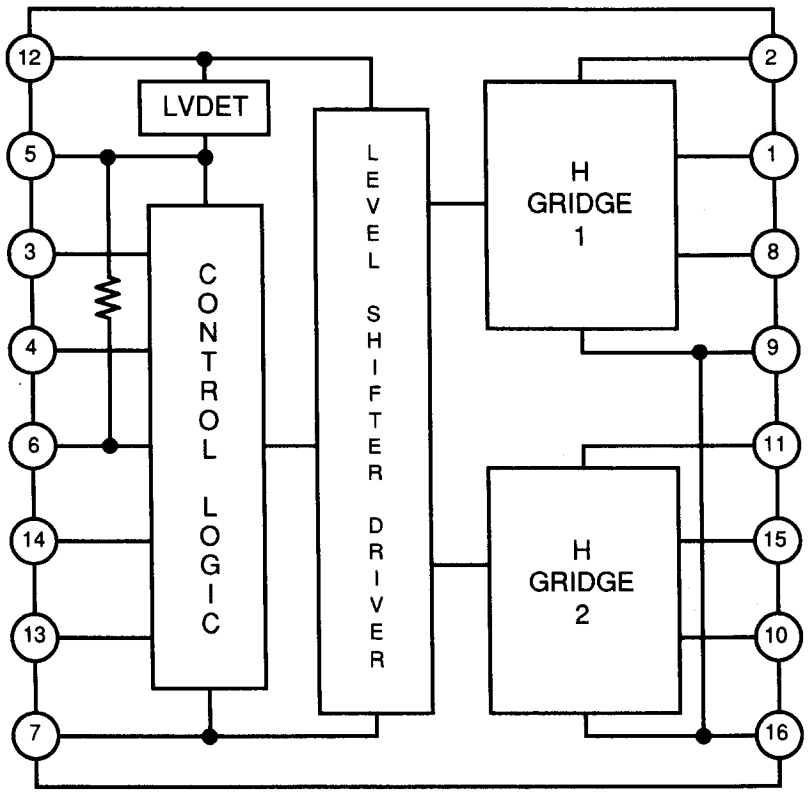


Table 2-5-3. Stepping Motor Driver Block Diagram

III. REPAIRS

1. Precautions for Repairs

(1) Incorporation of main board

The OPEN switch may break when the top cover is closed and the main board is incorporated after opening the main board and performing repairs. When the OPEN switch is broken, the state will become the same as power defect. (No displays and key inputs are accepted).

The main board can be incorporated smoothly by opening the top cover.

(2) Optical block

(i) Flexible board short-circuit by soldering

The optical block of the mini disc is easily damaged by static electricity. Therefore when removing it, solder and short-circuit the short-land on the flexible board.

After incorporation, be sure to desolder the short-circuit completely.

(ii) Laser power adjustment

The optical block and main board of the MZ-R3 have been adjusted at shipment so that they meet the standards. When replacing the optical block, the laser power adjustment need not be performed.

However, as the servo circuit has not yet been adjusted, after incorporating the optical block in the unit, perform the automatic adjustment of the servo circuit in the general test mode.

(3) Waveform Observation

(i) RF signal

To conserve power in the MZ-R3, the laser is turned off during intermittent reading when batteries are used. At this time, RF waveforms are not output.

When observing RF waveforms in the normal mode with batteries connected, RF waveforms may be generated or not generated repeatedly. This is normal.

When the AC adapter is connected, intermittent laser is not turned off.

(ii) S-Curve Waveform (FE Signal)

During the focus search of the mini disc, unlike the CD, the focus turns on when the objective lens moves away from the disc. Therefore, the focus does not turn on when the objective lens approaches the disc and the laser output is off.

All the S-curve output during focus search are waveforms for checking the P-P values and symmetry.

(Refer to Fig. 3-1-1.)

To observe this S-curve waveform, remove the R596 at the tip of the FE terminal (Pin 35 of IC501), and connect the test point 5460 at the side (RF amplifier side of R596) and VC to the oscilloscope. By performing focus search in this state, the S-curve waveform will be observed.

If the P-P value or symmetry of the waveform is abnormal, replace the optical block.

To observe this S-curve waveform, remove the R596 at the tip of the FE terminal (Pin 35 of IC501), and connect the test point 5460 at the side (RF amplifier side of R596) and VC to the oscilloscope. By performing focus search in this state, the S-curve waveform will be observed.

If the P-P value or symmetry of the waveform is abnormal, replace the optical block.

S-curve Waveform specification

- P-P value: 2.7 ± 0.1V
  (OK:the waveform is clipped above 2.8V)
- Symmetry:10: Abovr 5

S waveform for MD

- Symmetry (A:B or B:A) check
- P-P value check

Fig. 3-1-1. S-Curve Waveform of Mini Disc

(iii) Traverse Waveform (TE Signal)

The traverse waveform is automatically adjusted in the general test mode. If it cannot be performed properly, check with the traverse waveform.

If the P-P value and symmetry of the traverse waveform are abnormal, check that the signal is not disconnected (contact fault of flexible board, etc.) and replace the optical block.

Traverse signal

- P-P value: 2.45 ± 0.35V

2. Test Mode

(1) Outline

In the test mode, check of the servo circuit, audio circuit, and mechanism operations, and automatic adjustment of the servo circuit are performed.

(2) Setting the Test Mode

The MZ-R3 test mode can be set using the following two methods. When the test mode is set, the display changes. The test mode will take some time to set after the power is turned on.

- Short-circuit the test mode tap of the main board and connect the power supply.

(3) Exiting the Test Mode

Normally, the test mode can be exited by disconnecting the power supply. If adjustment faults occur in the automatic adjustment mode (general adjustment mode), this general adjustment mode will not be exited until the adjustment has been performed completely.

(Even if the power supply is disconnected, the general adjustment mode will be set again.)

When adjustment faults occur in the general adjustment mode, set the test mode again and perform repairs in the test mode circuit, etc. When the adjustment faults occur in the general adjustment mode, there is no need to return to the normal mode as the servo circuit is failure. (Servo circuit repairs should be given priority over those of the signal circuit.)

To return to the normal mode, open the top cover when the first display of the general adjustment mode is shown. "OF", "FO", "FF", etc. will be shown at the bottom right. This indicates adjustments OK/NG (right is CD and left is MO). When the FF or FR key is pressed, the display changes between 0 and F. Set to FF and disconnect the power supply. The normal mode will be returned.

However, as the adjustment has not been performed properly, be sure to repair the unit.

(4) Structure

When the test mode is set, the main mode will be set. In this main mode, all displays will repeatedly light and go off, and display the version.

The main mode is composed of the general adjustment mode and test mode. Pressing the FF key in the main mode sets the test mode and pressing the FR key sets the general adjustment mode.

- Test mode

Mode for performing adjustments and checks manually.

- General adjustment mode

Mode for performing automatic adjustments.

(5) Test Mode Details

For test mode details, refer to the SERVICE MANUAL.

3. OPERATIONS CHECK

(1) Checking in the General Adjustment Mode

Set the main mode, and press the FR key to set the general adjustment mode. In this mode, the automatic adjustment of the servo circuit will be performed. If the general adjustment mode indicates that both the CD and MO discs are normal, the servo circuit adjustment (checking in the manual test mode) need not be performed.

To execute the general adjustment mode, first check if the disc used is dirty, scratched, etc. Place the unit horizontally and make sure no shock or vibration will be imposed. (Never check holding it)

If problems occur during adjustments, NG will be displayed. Set the test mode again, press the FF key to set the manual test mode, and check and adjust the servo circuit.

(2) Checking in the Manual Test Mode (When general adjustment mode NG)

(i) Checking laser power

Using the laser power meter (LPM-8001), check the laser power output in the laser power check mode (21, 22).

If the output is small, check the laser current. If the laser current is large or small, it indicates that the laser diode has become weak. Therefore replace the optical block.

If no laser current flows, check the APC circuit of the main board.

(ii) Checking mechanism operations

(a) Sled tracking operations

Press the FF/FR key in the manual servo mode of the test mode (000) so that the optical block moves. Check that the sled moves smoothly.

If there are problems in the operations, check if there are foreign particles on the sled shaft and check the driver output.

Check that the sled operations can be performed normally even when the unit is placed on its side.

(However, as the conveyance spring of the optical block will become damaged, do not operate the unit without disc at the innermost and outermost circumferences.)

Check that the objective lens of the optical block moves in the tracking direction during the sled operations. If it does not, check for contact faults of the flexible board, driver output, etc.

(b) Focus search operations

Set the mode to 31 without loading any disc. Check that the objective lens performs the focus search operation smoothly.

If the operation is not normal, check the contact of the flexible board and driver output.

(iii) Checking servo circuit operations

(a) EF balance, ABCD, focus/tracking gain adjustments

If these adjustments are not properly performed, check the P-P value and symmetry of the S-curve waveform (FE signal) and traverse waveform (TE signal) and determine if the optical block is normal or not.

(b) Detrack tolerance (Mode 82:NG)

Mode 82 NG means the NG of the detrack tolerance check (Checking the ADIP error by swinging the laser spot to the left and right.)

However, mode 82 checks cannot be performed in the manual test mode.

If mode 82 is NG, check thoroughly for scratches and dirt on the disc. If NG occurs again, check using other disc. Also check if the unit is subjected to vibrations during adjustments. If NG persists, replace the optical block.

(Reference Information) Detrack Tolerance Check

The detrack tolerance check is checking for ADIP errors by shifting the E-F balance adjustment and shifting the laser spot on the groove slightly in the tracking direction. From this error, the optical block characteristics can be detected. If this check becomes NG, it indicates that the optical block characteristics have deteriorated. Therefore replace the optical block.

(c) BETA REC (Mode 63:NG)

The BETA REC CHECK NG means that the playback block error rate after BETA recording is more than 100/seconds (maximum 7350). Therefore, it indicates that the servo circuit, recording circuit, or playback circuit is faulty.

Load a test disc recorded with linking data (BETA REC completed disc) in the unit. Move the optical block to the 300th to 700th cluster recording with the linking data and set to mode 39 in order to check the error rate of the playback circuit only. (The error rate cannot be measured in normally recorded disc.) If the playback error rate is normal, the servo circuit and playback circuit can be determined as normal (recording circuit fault).

- Disc recorded with linking data (PTDM-001)
  ..... P/N J-2501-054-A

(Note)Setting mode 39

To set mode 39, set mode 30 and press the PLAY key once.Wait for mode 31 to become mode 32 automatically and press the PLAY key again.

Don't Press the PLAY key quickly following mode 30. Take note that the all servo ON mode will not be set even if mode 39 is displayed in this case.

When the all servo on state is set and the disc data can be read in mode 39, the address of the disc (cluster number) is displayed in hexadecimal 3 digits on the display.

The hexadecimal 2 digits on the right indicate the AT error rate (ADIP signal reading error) and the hexadecimal 2 digits at the right edge indicate the block error rate (EFM signal reading error).

Therefore, if the block error rate at the right edge is above 100 (64 in hexadecimal), it indicates that BETA REC is NG. It is NG even when the AT error rate is above 3.

- When the playback error rate is abnormal
  - Check the playback position of the optical block (What are the positions of clusters 300 to 700?)
  - Focus ON check (Does mode 31 change to mode 32 automatically?)
  - Servo circuit adjustment re-check (Servo circuit checking)

- When the playback error rate is normal (Recording circuit NG)
  - Temperature compensation check
    Compare the temperature displayed for mode 16 and the room temperature. If more than ± 5 °C difference, replace IC504.
    (The unit will warm up when power is connected and display a higher temperature than the room.)
  - Laser emission check (Laser power)
  - Magnetic head output check (REC board HA, HB output)

(3) Other checks

(i) Audio circuit (played back sounds)

In the audio mode (mode 100) of the manual test mode, the 1 kHz, 0dB sine wave is output from the ATRAC (IC601) from the system control (IC601).

By using this sine wave, circuits after the D/A converter (IC304) can be checked.

(ii) Mechanism mode change

The mechanism operations of the stepping motor can be checked in the mechanism mode (Mode 200. But 2 will not be displayed) of the manual test mode.

(iii) Power supply differentiation and charge circuit

In the power supply mode of the manual test mode (Mode 300. However 3 will not be displayed.), the power detection circuit and charge circuit can be checked.

When mode 310 is set and the PLAY key is pressed, the connected power supply is automatically differentiated and displayed.

When mode 320 is set and the PLAY key is pressed, charge conditions (DC power supply and rechargeable battery connection) are checked. If the conditions are satisfied, charge operations are started.

4. TROUBLESHOOTING

(1) Power supply faults

(i) The unit does not start (No display)

a. Check start-up with each power supply

(Cause) The lead wire of the rechargeable battery case is broken

The rechargeable battery is faulty

6V AC adapter is incorrectly inserted

b. Check the UNREG voltage (UNMNT Pin 59 of IC801)

(Cause) The AC jack contact is faulty

THP901 is faulty

c. Check the MICON+B voltage (VOUT Pin 5 of IC802)

(Cause) The microprocessor power supply (IC802, etc.) is faulty

d. Check the OPEN switch input (when switch is broken, no display, etc.)

(Cause) The S817 (OPEN) switch is broken...Pay attention when incorporating in the main unit

e. Check key inputs (Pins 55 to 58 of IC801)

(Cause) Incorrect key inputs due to faulty switch

f. Check PCONT signal and display inputs/outputs

(Cause) Q803 is faulty

CN802 contact is faulty

(ii) The battery cannot be charged

a. Check the rechargeable battery voltage after charging

(Cause) The rechargeable battery is faulty

The charge circuit is faulty

b. Check the AC adapter connection

(Cause) S901 (AC/EXT) is faulty

The AC jack contact is faulty

c. Check the UNREG voltage

(Cause) THP901 is faulty

d. Check the rechargeable battery detection

(Cause) S902 (AM3/NI) is faulty

e. Check the charge circuit

(Cause) Q904, Q906 is faulty

IC901 is faulty

(2). Faulty Playback Operations

(i) TOC cannot be read (Disc Error)

a. Check sled operations (Internal circumference access of optical block)
   (Cause) The sled related mechanism is faulty

b. Check the laser power
   (Cause) The laser diode has deteriorated
   The objective lens is dirty, etc.

c. Check focus search operations
   (Cause) The flexible board contact is faulty
   The optical block is faulty

d. Check tracking coil operations
   (Cause) The flexible board contact is faulty

e. Check the RF waveform (P-P value, up/down vibration)
   (Cause) Electrical adjustments were not performed properly
   The optical block is faulty
   Foreign particles on the spindle motor

f. Check traverse adjustments, etc.
   (Cause) The optical block is faulty
   The flexible board contact is faulty

(ii) Sound skip, sound stop, noise

a. Headphone check
   (Cause) The jack contact is faulty
   The headphone is faulty

b. Check for digital noises (machine-gun noise, humming sounds)
   (Cause) ATRAC (IC601) is faulty

c. Check the assembly of unit (If playback stops when unit is subjected to shock.)
   (Cause) The flexible board is not mounted completely, the flexible board contact is faulty.
   The connector lock is faulty

d. Tilt the unit and check changes in the RF waveform (P-P value, clearness of waveform)
   (Cause) The optical block is faulty

e. Check aging
   (Cause) The disc is scratched
   Foreign particles on the sled

(3). Faulty Recording Operations

(i) No recording

a. Check playback operations

(Cause) The servo circuit is faulty

b. Check laser power

(Cause) The laser power has not been adjusted properly

The laser diode has deteriorated

Foreign particles on the objective lens

c. Check the magnetic head state

(Cause) The magnetic head is broken or bent

d. Check the recording signal line

(Cause) The flexible board is broken or contact is faulty

(ii) Sound skip, tracking-mark errors during digital recording

a. Check the input source (Check on other digital equipment)

(Cause) The CD player is old (No tracking-marks as the signal output version is old)

Track-markings are not provided during repeated playing of the same song (Unit specifications)

Example:3rd song → 3rd song → 3rd song

When the disc is changed by the CD changer, if the same track number is played, tracking-marks are not provided. (Unit specifications)

Example:3rd song of 1st disc → 3rd song of 2nd disc

Digital optical output waveform error at transmission equipment side

b. Check the tracking-mark (Check with other MZ-R3)

(Cause) The optical jack contact is faulty

Appendix

1. Pin Functions of System Controller (IC801)

No.	Pin Name	I/O	Function
1	CLLS	O	Chip select output of IC804 (clock)
2	XRST	O	Reset signal output of IC. L:Reset
3	WRPWR	O	Laser power switching output to CXD2535 H:Recording power
4	TX	O	Write data transmission enable output to CXD2536
5	SENSE	I	SENSE signal input from CXD2535, CXD2536
6	LDON	O	Laser diode emission signal output. H:Emission
7	XSHOCK	I	Recording shock detection input from CXD2535
8	FOK	I	Focus OK signal input from CXD2535
9	INLS	I	Input of optical block moving completion to innermost circumference
10	PROTECT	I	Disc rec-proof switch input. H:Protected
11	AVLSI/DATA	I/O	AVLS input/remote control LCD data output R3:AVLSI.E3:DATA.
12	HOLD	I	HOLD switch input. L:HOLD
13	WP	I	Wake-up signal input L:Start-up from sleep mode
14	OPEN	I	OPEN switch input. L:Closed
15	AM3/NI	I	Dry battery/Ni-MH rechargeable battery detection switch input L:Ni-MH
16	CLSDIO	I/O	Serial data input/output for IC804 (Clock)
17	SDIO2	I/O	Serial data input/output with NV RAM, EVR
18	DSP-RS	I/O	Display register selection
19	DSP-RW	I/O	Display data read/write
20	DSP-E	I/O	Display data enable
21	DB7	O	Display data
22	DB6	O	Display data
23	DB5	O	Display data
24	DB4	O	Display data
25	DB3	O	Display data
26	DB2	O	Display data

27	DB1	O	Display data
28	DB0	O	Display data
29	MON/ST	O	Monaural/stereo mode selection signal output
30	PCONT	O	Power control signal output. L:Start-up
31	BATTON	O	Detection voltage shift output when batteries are used L:Battery voltage is below 2.5V
32	RECLED	O	Recording LED lighting signal output. L:Lit
33	MODE2	O	Recording driver mode setting output
34	MODE1	O	Recording driver mode setting output
35	RFSW	O	RF amplifier power selection output when batteries are used L:Power supply is off
36	CSREC	O	Recording control (IC315) latch signal output
37	MP	—	Connected to GND
38	MRST	I	Reset input
39	VSS	—	GND
40	XTAL	—	System clock (12 Mhz) connection terminal
41	EXTAL	—	System clock (12 MHz) connection terminal
42	CS	—	Connected to MICON+B
43	SDIO	I	Not used. Connected to GND
44	SDDO	O	Serial data output to CXA1381, LCD driver
45	SCKO	O	Serial clock output to CXA1381, LCD driver
46	MODE	I	Test mode setting input
47	FDMON	I	Focus coil drive voltage monitor input
48	CLSCK	O	Serial clock output to IC804 (Clock)
49	KEY2	I	Remote control key input
50	AVSS	—	A/D converter GND
51	AVREF	—	A/D converter reference voltage
52	AVDD	—	A/D converter VDD
53	AC/EXTBAT	I	Lithium ion rechargeable battery connection detection input. L:External battery
54	CLOCK	I	CLOCK key input
55	PLAYKEY	I	PLAY key input
56	RECKEY	I	REC key input

57	KEY0	I	Main key inputs
58	KEY1	I	LCD unit internal key inputs
59	UNMNT	I	UNREG voltage monitor input
60	BATTMNT	I	Rechargeable battery voltage monitor input
61	FGIN	I	FG input from motor driver (IC701)
62	SLA	I	Character input dial input
63	SLB	I	Character input dial input
64	INTSW	I	Mechanism mode detection input
65	PACKIN	I	Disc presence detection input. L:Disc present
66	JACKDET	I	Optical/line jack inserted detection. L:Jack is inserted
67	OPTDET	I	Optical jack detection. H:Optical jack
68	MICDET	I	Mic inserted detection. L:Mic is inserted
69	XLAT	O	CXD2535, 2536 serial-data latch signal output
70	KEYON	O	Remote control key wake-up detection setting output. L:During Sleep
71	ST1SOU	O	Stepping motor control output
72	ST2SOU	O	Stepping motor control output
73	CHGCONT	O	Charge current control output
74	XLATRF	O	Serial data communication latch output to CXA1381
75	DQSY	I	Digital IN input sub-code Q sync signal input
76	TCOUNT	I	Playback power output:Track count input Recording power output:Shock input
77	SDI1	I	CXD2535, 2536 serial data input
78	SDO1	O	CXD2535, 2536 serial data output
79	SCK1	O	CXD2535, 2536 serial clock output
80	SQSY	I	Sub-code Q/ADIP sync signal input
81	BEEP	O	Beep sound control output. H:Beep sound output
82	FBP	O	Focus bias voltage output (PWM output during power ON)
83	REFLCT	I	Disc reflectivity detection switch input
84	TEX	—	Not used. Connected to GND
85	XT	—	Not used
86	VSS	—	GND terminal

87	VDD	—	Power supply terminal
88	NC	—	Not used
89	DEEMP	O	De-emphasis switching output. L:Deemphasis ON
90	PDDA	O	D/A converter power-down output during recording H:Power down
91	PDAD	O	A/D converter power-down output during playback H:Power down
92	OUTSEL	O	Recording audio circuit power cut output H:During playback. L:During recording
93	AMUTE	O	Analog mute signal output. L:Muted
94	OPTCONT	O	Optical input photo detector power supply control output H:During recording. L:During playback
95	CSHP	O	Headphone control chip select output
96	CSNV	O	NV RAM chip select output
97	SCK2	O	Serial clock output to NV RAM, EVR
98	AGC	O	AGC automatic/manual selection output
99	SHCKEN	O	Shock detection enable output
100	CHG	O	Charge operation control output. H:Charge

2. RF Amplifier (IC501, CXA1981AR)

SONY

CXA1981R

RF MATRIX AMPLIFIER FOR MD

Outline

The CXA1981R processes the RF signals used for recording and playing back the Minidisc.
It has been designed for use together with the CXD2535AR.

Features

- RF matrix amplifier suitable for the digital servo processor
- Can be used for both the Minidisc recorder and player
- Mode selection with serial interface

Functions

- Pit/groove selection RF amplifier
  (With AGC, equalizer function)
- Focus bias adjustment 3T detection output
- Gain selection I-V amplifier
- Light amount signal output/peak hold output/bottom hold output
- Focus error signal output
- Tracking error signal output
- EF balance adjustment gain selection switch
- Sled error signal output
- ADIP binary output
- VREF output
- APC PD amplifier
- Temperature sensor amplifier

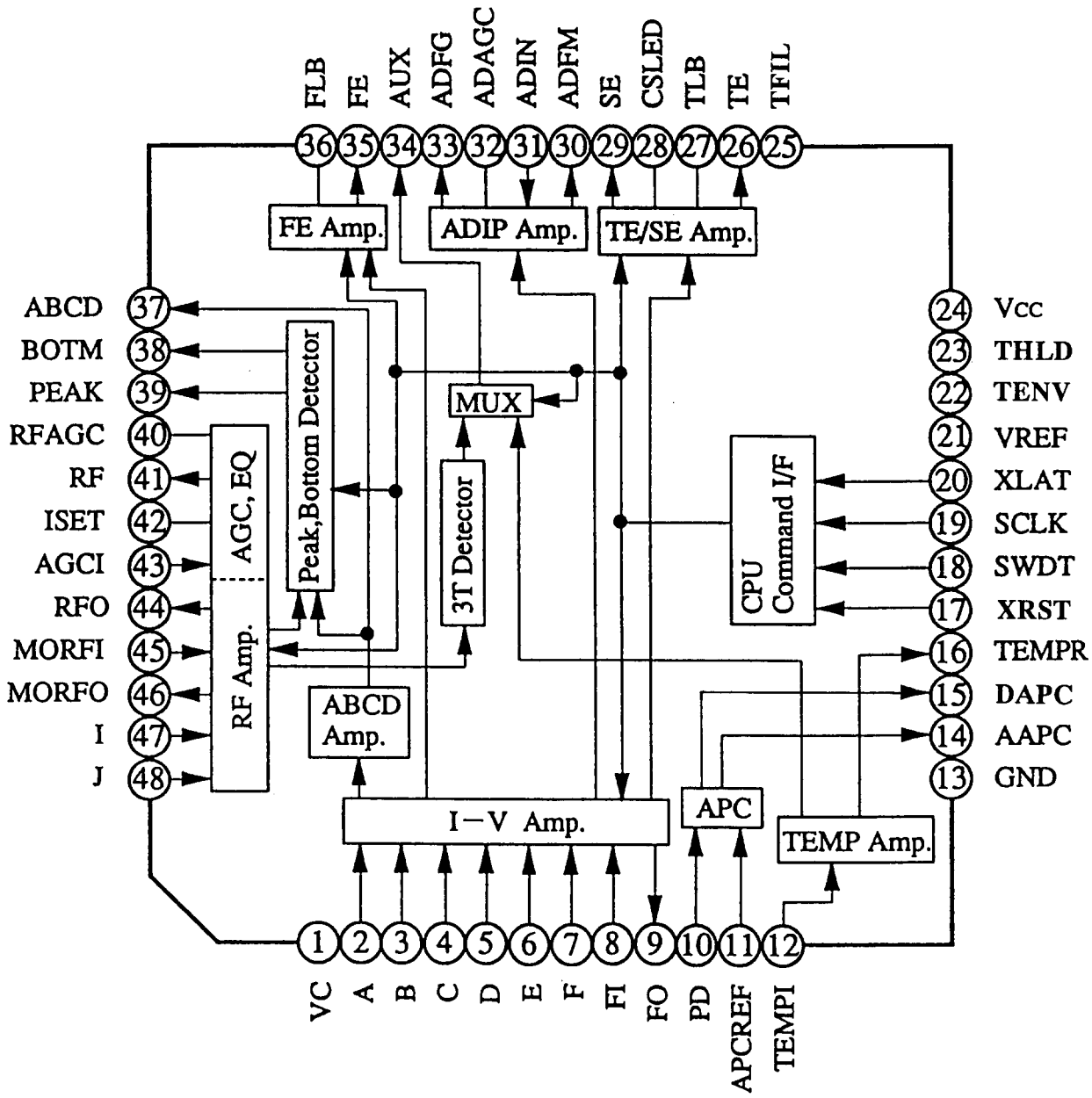
Purpose

Minidisc recorder/player

Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration



Pin Functions

Pin No.	Symbol	I/O	Function
1	VC	O	VCC/2 voltage output pin.
2	A	I	Main beam servo signal A current input pin.
3	B	I	Main beam servo signal B current input pin.
4	C	I	Main beam servo signal C current input pin.
5	D	I	Main beam servo signal D current input pin.
6	E	I	Main beam servo signal E current input pin.
7	F	I	Main beam servo signal F current input pin.
8	FI	I	EF balance adjustment pin.
9	FO	O	EF balance adjustment pin
10	PD	I	Light amount monitor signal input pin.
11	APCREF	I	Laser power setting reference voltage input pin.
12	TENPI	I	Temperature sensor connection pin.
13	GND	—	GND pin.
14	AAPC	O	Analog APC output pin.
15	DAPC	O	Digital APC output pin.
16	TEMPR	O	Temperature sensor reference voltage output pin.
17	XRST	I	Reset signal input pin. (L: Reset)
18	SWDT	I	Microprocessor serial interface data input pin.
19	SCLK	I	Microprocessor serial interface shift clock input pin.
20	XLAT	I	Microprocessor serial interface latch input pin. Latched at "L".
21	VREF	O	Reference voltage output pin.
22	TENV	O	Tracking envelope signal output pin.
23	THLD	—	Track hold capacitor connection pin.
24	VCC	—	Power supply pin.
25	TFIL	I	Track hold input pin.
26	TE	O	Tracking error signal output pin.
27	TLB	—	Tracking error signal low boost capacitor connection pin.
28	CSLED	—	Sled error signal LPF capacitor connection pin.
29	SE	O	Sled error signal output pin.
30	ADFM	O	ADIP FM signal output pin.
31	ADIN	I	ADIP signal comparator input pin.
32	ADAGC	—	ADIP AGC capacitor connection pin.
33	ADFG	O	ADIP binary signal output pin.
34	AUX	O	I3 output/temperature signal output pin.
35	FE	O	Focus error signal output pin.
36	FLB	—	Focus error signal low boost capacitor connection pin.
37	ABCD	O	Main beam servo detector light amount signal output pin.
38	BOTM	O	RF/ABCD bottom signal output pin.
39	PEAK	O	RF/ABCD peak signal output pin.
40	RFAGC	—	RF AGC capacitor connection pin.

Pin No.	Symbol	I/O	Function
41	RF	O	RF equalizer output pin.
42	ISET	—	BPF (f0 = 720 kHz, 22 kHz) and RF equalizer setting pin.
43	AGCI	I	RF AGC input pin.
44	RFO	O	RF amplifier output pin. Eye-pattern check point.
45	MORFI	I	Pin input with AC-linked groove RF signal.
46	MORFO	O	Groove RF signal output pin.
47	I	I	I-V converted RF signal I input pin.
48	J	I	I-V converted RF signal J input pin.

3. Digital Servo (IC503, CXD2535BR)

SONY CXD2535BR

EFM/ACIRC Encoder/Decoder with Built-In Digital Servo Processor for Minidisc

Outline

The CXD2535AR is a EFM/ACIRC encoder/decoder with built-in digital servo processor. It was designed for use with the CXA1981R.

Functions, Features

- EFM encode/decode
- ACIRC encode/decode
- EFM comparator
- ADIP decode
- EFM digital PLL
- BUilt-in Encoder PLL VCO
- Built-in error correction RAM
- Highly efficient error correction function
  (Cl : Double correction, C2 : Quadruple correction)
- Digital in/out
- Peak level detection
- Digital servo
  (Focus, tracking, sled, spindle)
- Servo AGC
- Servo auto sequencer
- Servo system adjustment using microprocessor
- System gain function
- High speed microprocessor interface

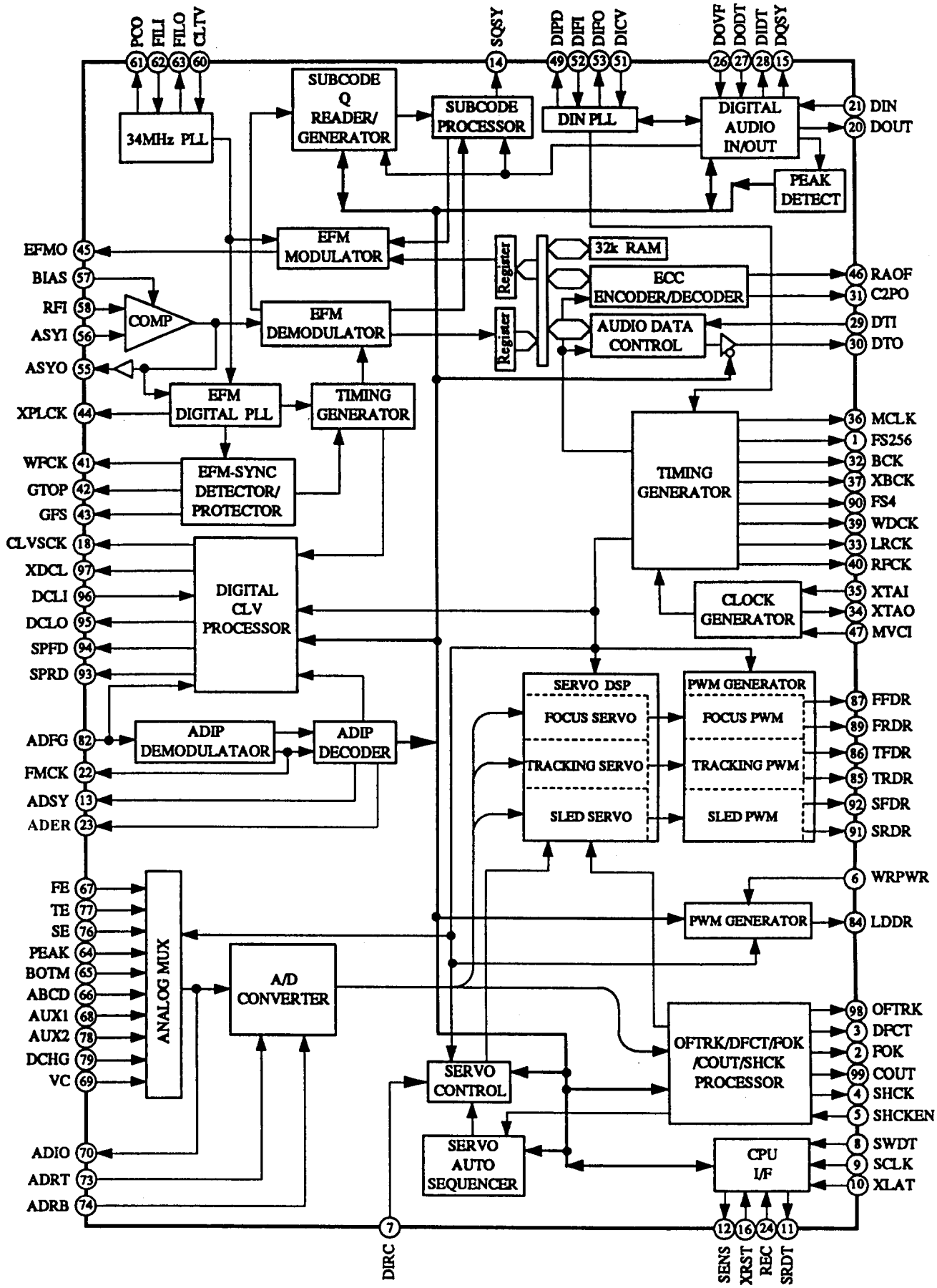
Structure

Silicon gate CMOS

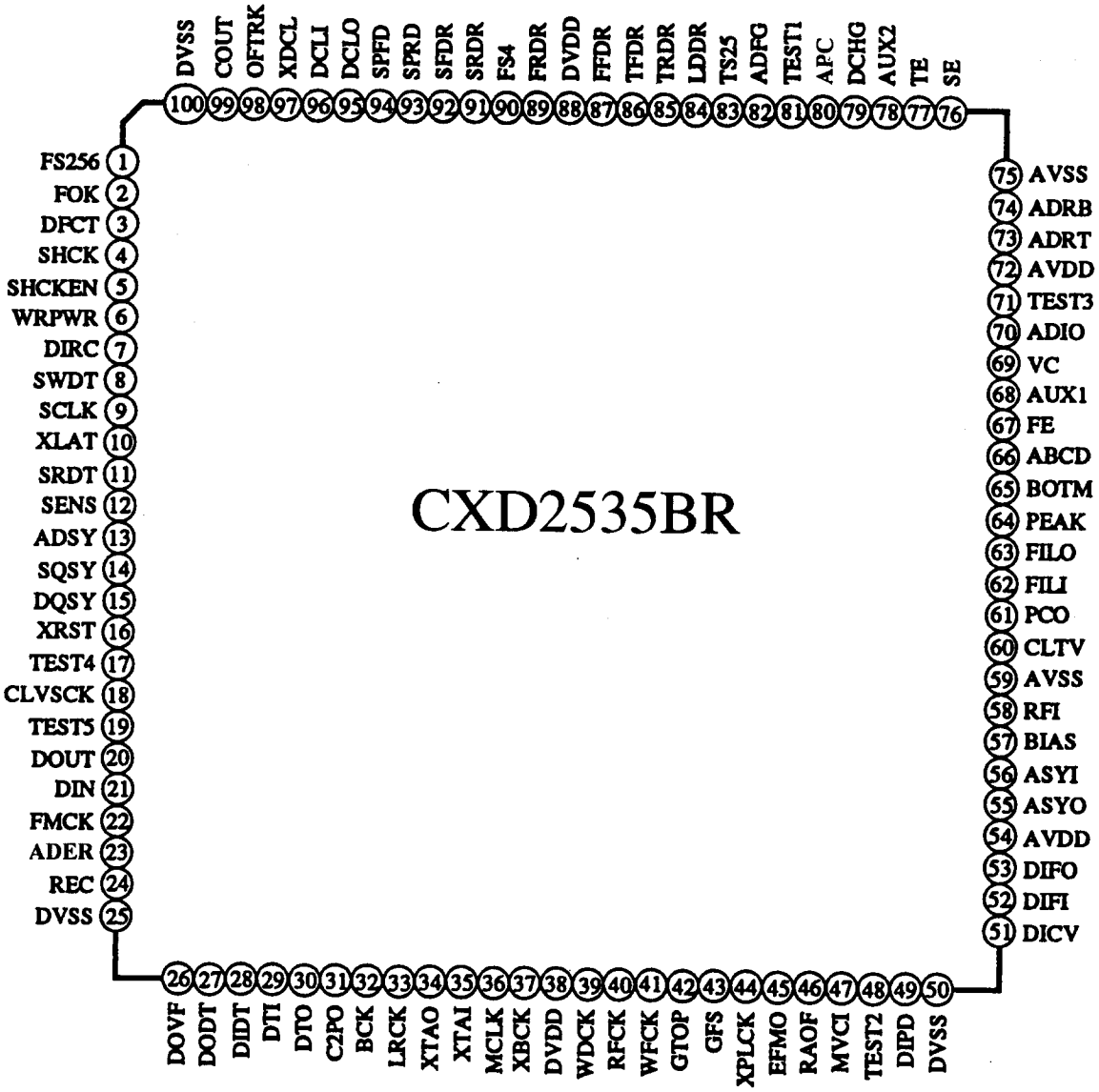
Purpose

Minidisc recorder/player

Block Diagram



Pin Configuration



Pin Functions

Pin No.	Pin Name	I/O		Function
1	FS256	O	H, L	256 Fs output (11.2896 MHz).
2	FOK	O	H, L	Focus OK signal output. Focus OK when "H".
3	DFCT	O	H, L	Defect detection output. Defect when "H".
4	SHCK	O	H, L	Track jump detection output.
5	SHCKN	I		Track jump detection enable input. Enable when "H".
6	WRPWR	I		Laser power selection input. Recording power when "H". Playback power when "L".
7	DIRC	I		Track jump control signal.
8	SWDT	I		Microprocessor serial interface data input.
9	SCLK	I		Microprocessor serial interface shift clock input.
10	XLAT	I		Microprocessor serial interface latch input. Latched at falling edge.
11	SRDT	O	H, Z, L	Microprocessor serial interface data output.
12	SENS	O	H, Z, L	Outputs internal status according to the micro serial interface address.
13	ADSY	O	H, L	ADIP sync output.
14	SQSY	O	H, L	Disc sub-code Q sync/ADIP sync output.
15	DQSY	O	H, L	When the digital-in source is CD or MD. Ubit CD or MD format sub-code Q sync output.
16	XRST	I		Reset input. Reset when "L".
17	TEST4	I		Test pin. Connect to GND.
18	CLVCK	O	H, L	Spindle servo evaluation clock output (5.6448 MHz).
19	TEST5	I		Test pin. COnnect to GND.
20	DOUT	O	H, L	Digital audio interface signal output.
21	DIN	I		Digital audio interface signal input.
22	FMCK	O	H, L	ADIP FM demodulation clock output.
23	ADER	O	H, L	ADIP CRC flag output. Error when "H".
24	REC	I		Recording/playback selection. Recording when "H". PLayback when "L".
25	DVSS	I		Digital GND.
26	DOVF	I		Vbit input of signal output from DOUT pin.
27	DODT	O		Signal output from DOUT pin and audio data input for peak level detection.
28	DIDT	I	H, L	Audio data output of signal input from DIN pin.
29	DTI	O		Recording data input from CXD2536A.
30	DTO	O	H, Z, L	Playback data output to CXD2536A in playback. "Z" during recording.
31	C2PO	O		Outputs the C2 pointer of played back data during playback. During Digital Rec, outputs the Vbit of digital-in. "L" during Analog Rec.
32	BCK	O	H, L	64Fs output (2.8224 MHz).
33	LRCK	O	H, L	Fs output (44.1 kHz).
34	XTAO	I	H, L	Crystal oscillation circuit output pin (XTAI pin inversion output).
35	XTAI	O	H, L	Crystal oscillation circuit input pin (512Fs = 22.5792 MHz).
36	MCLK	O	H, L	Master clock output (512 Fs = 22.5792 MHz).
37	XBCK	O	H, L	BCK inversion output.

Pin No.	Pin Name	I/O		Function
38	DVDD			Digital power supply.
39	WDCK	O	H, L	2 Fs output (88.2 kHz).
40	RFCK	O	H, L	Read frame clock output (Fs/6).
41	WFCK	O	H, L	Write frame clock output. Frame sync protection window operating state monitor.
42	GTOP	O	H, L	Frame sync protection window is released when "H".
43	GFS	O	H, L	Frame sync OK when "H".
44	XPLCK	O	H, L	EFM decoder PLL clock output (98Fs = 4.3218 MHz).
45	EFMO	O	H, L	"L" during playback. EFM (Encode data) is output during recording.
46	RAOF	O	H, L	RAM overflow output during playback.
47	MVCI	I		Digital-in PLL external VCO clock input.
48	TEST2	I		Test pin. Connect to GND.
49	DIPD	O	H, Z, L	Digital-in PLL phase comparison output.
50	DVSS			Digital GND.
51	DICV	I	Analog	Digital-in PLL internal VCO control voltage input.
52	DIFI	I	Analog	Filter input when digital-in PLL internal VCO is used.
53	DIFO	O	Analog	Filter output when digital-in PLL internal VCO is used.
54	AVDD			Analog power supply.
55	ASYO	O	H, L	Playback EFM full-swing output ("L" = VSS. "H" = VDD).
56	ASYI	I	Analog	Playback EFM comparator slice voltage input.
57	BIAS	I	Analog	Playback comparator bias current input.
58	RFI	I	Analog	Playback EFM RF signal input.
59	AVSS			Analog GND,
60	CLTV	I	Analog	Internal VCO control voltage input for recording EFM PLL and playback digital PLL master PLL.
61	PCO	O	H, Z, L	Phase comparison output for recording EFM PLL and playback digital PLL master PLL.
62	FILI	I	Analog	Filter input for recording EFM PLL and playback digital PLL master PLL.
63	FILO	O	Analog	Filter output for recording EFM PLL and playback digital PLL master PLL.
64	PEAK	I	Analog	Light amount peak hold signal input.
65	BOTM	I	Analog	Light amount bottom hold signal input.
66	ABCD	I	Analog	Light amount signal input.
67	FE	I	Analog	Focus error signal input.
68	AUX1	I	Analog	Auxiliary input 1.
69	VC	I	Analog	Mid-point voltage input.
70	ADIO	O	Analog	A/D converter input signal monitor output.
71	TEST3			Test pin. Connect to GND.
72	AVDD			Analog power supply.
73	ADRT	I	Analog	A/D converter operating range upper limit voltage input.
74	ADRB	I	Analog	A/D converter operating range lower limit voltage input.

Pin No.	Pin Name	I/O		Function
75	AVSS			Analog GND.
76	SE	I	Analog	Sled error signal input.
77	TE	I	Analog	Tracking error signal input.
78	AUX2	I	Analog	Auxiliary input 2.
79	DCHG	I		Connect to GND.
80	APC	I	Analog	Laser APC input pin.
81	TEST1	I		Test pin. Connect to GND.
82	ADFG	I		ADIP binary FM signal (22.05 ± 1 kHz) input.
83	TS25	I		Test pin. Connect to GND.
84	LDDR	O	H, L	Laser drive output.
85	TRDR	O	H, L	Tracking servo drive output. (–)
86	TFDR	O	H, L	Tracking servo drive output. (+)
87	FEDR	O	H, L	Focus servo drive output. (+)
88	DVDD			Digital power supply.
89	FRDR	O	H, L	Focus servo drive output. (–)
90	FS4	O	H, L	4 Fs output (176.4 kHz).
91	SRDR	O	H, L	Sled servo drive output. (–)
92	SFDR	O	H, L	Sled servo drive output. (+)
93	SPRD	O	H, L	Spindle servo drive output. (–)
94	SPFD	O	H, L	Spindle servo drive output. (+)
95	DCLO	O	H, L	Spindle servo evaluation serial data output.
96	DCLI	I		Spindle servo evaluation serial data input.
97	XDCL	O	H, L	Spindle servo evaluation serial data load signal output.
98	OFTRK	O	H, L	Off-track signal output. Off-track when "H".
99	COUT	O	H, L	Track jump number count signal output.
100	DVSS			Digital GND.

* DIRC pin : Used when performing track jump without using the auto sequencer.
* When the auto sequencer is not used, set to "H".
* A feedback resistor is incorporated between the XTAI and XTAO pins.
* GFS pin : When the frame sync and interpolation protection timing match, it is set to "H".
* RAO pin : During playback, the internal 32k RAM exceeds the ±4 frame jitter margin, it becomes "H".
* MVCI pin : When an internal VCO is used in the digital PLL, connect to the GND.
* DICV pin : When the external VCO is used in the digital-in PLL, set to "H".
* Connect DCHG pin to the low impedance GND.
* AUX1, AUX2 pins:When not used, connect to the GND.
* The C2PO pin cannot be error corrected when "H" in playback.

Reset timing when power is on

When the power is turned on and when more than 10 master clocks have been input to the XTAI pin, the XRST pin becomes "H" from "L".

Note) To reset, when the XRST pin is "L", it is necessary to input more than 10 master clocks to the XTAL pin.

4. ATRAC (IC601, CXD2536R)

SONY CXD2536R

ACRAC Encoder/Decoder with Built-In Memory Controller for Minidisc

Outline

The CXD2536R is a LSI which encodes/decodes the memory control and audio compression ATRAC (Adaptive TRansform Acoustic Coding).

Functions, Features

- Reduced microprocessor software load with new command system
- ATRAC high sound quality algorithm
  Digital in/out 20 bits, analog in/out 24 bits
- Rich memory access function
- External RAM address space
  DRAM : 16 Mbit (Max.)

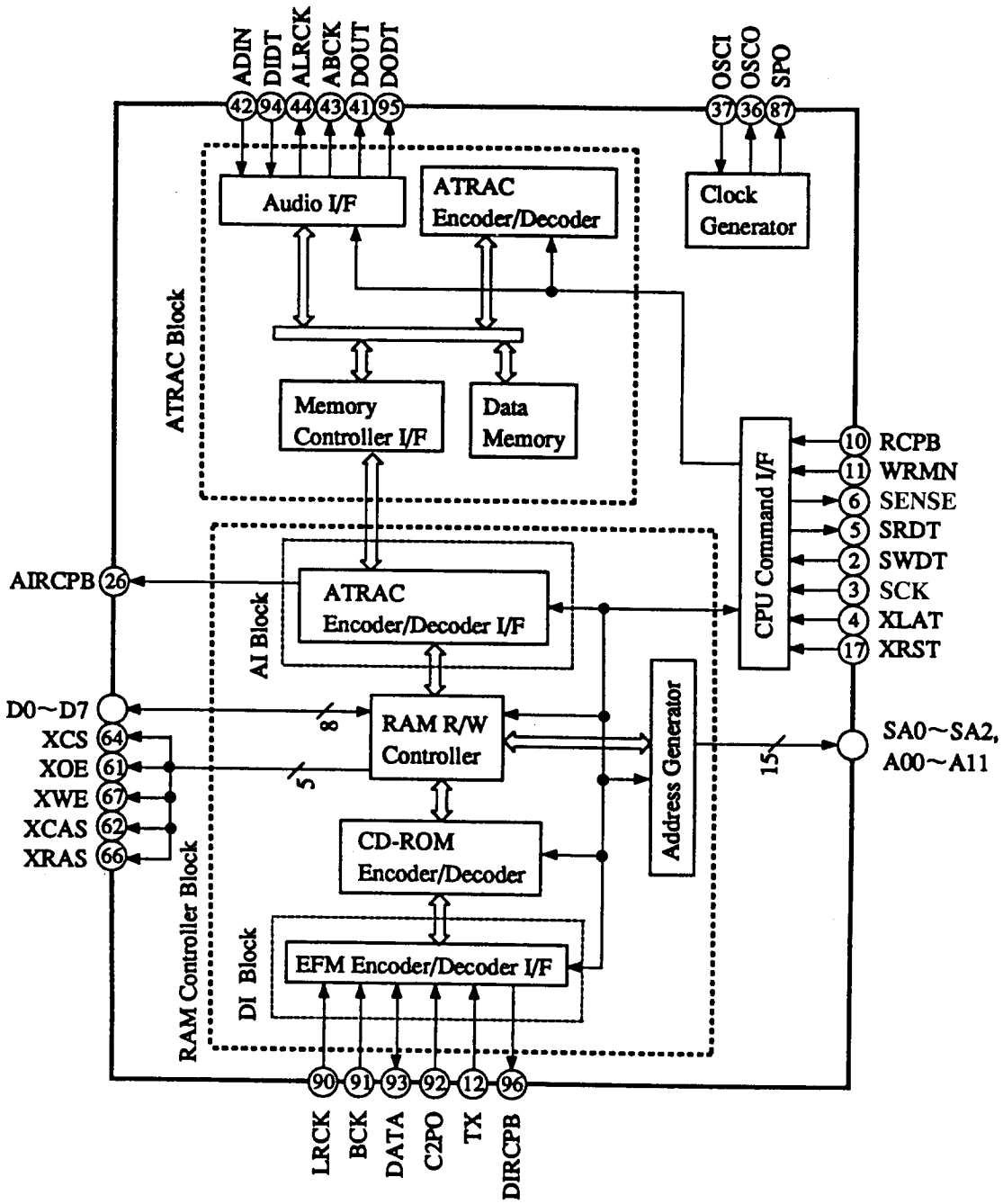
Structure

Silicon gate CMOS

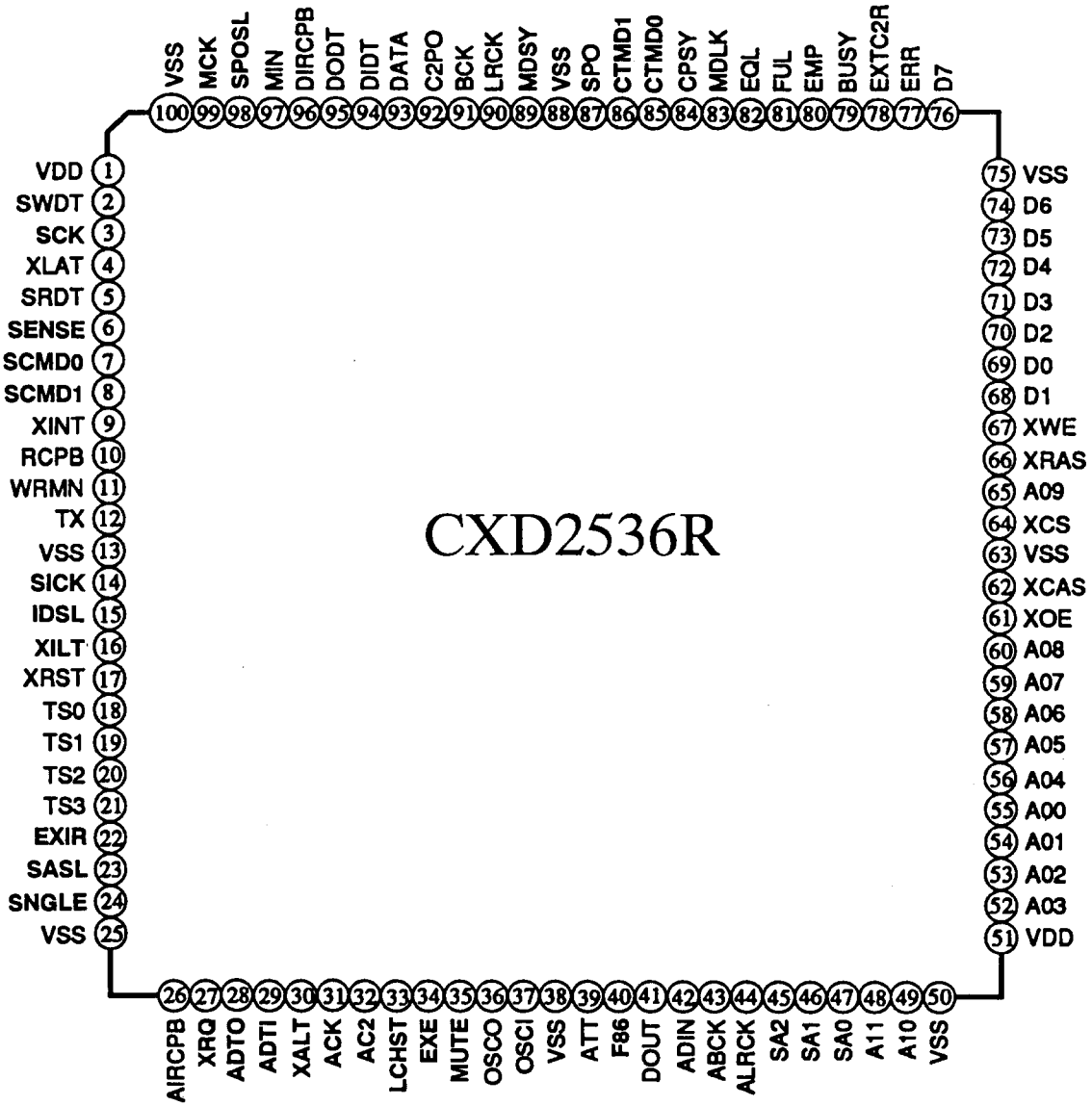
Purpose

Minidisc recorder/player

Block Diagram



Pin Configuration



Pin No.	Pin Name	I/O		Function
1	VDD			Power supply pin.
2	SWDT	I		Microprocessor serial interface data input.
3	SCK	I		Microprocessor serial interface shift clock input.
4	XLAT	I		Microprocessor serial interface latch input. Latched at falling edge.
5	SRDT	O	H, Z, L	Microprocessor serial interface data output.
6	SENSE	O	H, Z, L	Outputs internal status according the micro serial interface address.
7	SCMD0	I		Serial command control mode.
8	SCMD1	I		Serial command control mode.
9	XINT	O	H, L	Interrupt request output pin. Becomes "L" when interrupt status is generated.
10	RCPB	I		"H" recording mode/"L" playback mode.
11	WRMN	I		"H" write mode/"L" monitor mode.
12	TX	I		Recording data output enable signal input pin. Enabled at "H".
13	VSS			Connect to GND.
14	SICK	I		
15	IDSL	I		
16	XILT	I		
17	XRST	I		Reset input. Reset at "L".
18	TS0	I		Test pin. Connect to GND.
19	TS1	I		Test pin. Connect to GND.
20	TS2	I		Test pin. Connect to GND.
21	TS3	I		Test pin. Connect to GND.
22	EXIR	I		
23	SASL	I		Selects block in single use.
24	SNGLE	I		L: Normal use. H: Single use as ATRAC or RAM controller
25	VSS			Connect to GND.
26	AIRCPB	O	H, L	ATRAC block recording/playback mode output. When "H", recording mode. When "L", playback mode.
27	XRQ	I/O		ATRAC I/F XRQ input/output.
28	ADTO	I/O		ATRAC decode data input/output.
29	ADTI	I/O		ATRAC encode data input/output.
30	XALT	I/O		ATRAC I/F XALT input/output.
31	ACK	I/O		ATRAC I/F ACK input/output.
32	AC2	I/O		ATRAC I/F error data input/output.
33	LCHST	I/O		ATRAC I/F Lch start data input/output.
34	EXE	I/O		ATRAC I/F EXE input/output.
35	MUTE	I/O		ATRAC I/F MUTE input/output.
36	OSCO	O		Crystal oscillation circuit output pin (1024 Fs).
37	OSCI	I		Crystal oscillation circuit input pin (1024 Fs).
38	VSS			COnnect to GND.
39	ATT	I/O		ATRAC I/F ATT input/output.

Pin No.	Pin Name	I/O		Function
40	F86	O		ATRAC block 11.6 ms timing output.
41	DOUT	O	H, L	REC monitor output/decode audio data output.
42	ADIN	I		Analog recording input pin (Connected to external A/D converter).
43	ABCK	O	H, L	Outputs XBCK (64 Fs) to the external audio block.
44	ALRCK	O	H, L	Outputs LRCK (Fs) to the external audio block.
45	SA2	O	H, L	SRAM address bus.
46	SA1	O	H, L	SRAM address bus.
47	SA0	O	H, L	SRAM address bus.
48	A11	O	H, L	RAM address bus.
49	A10	O	H, L	RAM address bus.
50	VSS			Connect to GND.
51	VDD			Power supply pin.
52	A03	O	H, L	RAM address bus.
53	A02	O	H, L	RAM address bus.
54	A01	O	H, L	RAM address bus.
55	A00	O	H, L	RAM address bus.
56	A04	O	H, L	RAM address bus.
57	A05	O	H, L	RAM address bus.
58	A06	O	H, L	RAM address bus.
59	A07	O	H, L	RAM address bus.
60	A08	O	H, L	RAM address bus.
61	XOE	O	H, L	RAM output enable.
62	XCAS	O	H, L	DRAM $\overline{\text{CAS}}$ output.
63	VSS			Connect to GND.
64	XCS	O	H, L	RAM chip select. "H": DRAM. "L": SRAM.
65	A09	O	H, L	RAM address bus.
66	XRAS	O	H, L	DRAM $\overline{\text{RAS}}$ output.
67	XWE	O	H, L	RAM write enable.
68	D1	I/O	H, L	RAM data bus.
69	D0	I/O	H, L	RAM data bus.
70	D2	I/O	H, L	RAM data bus.
71	D3	I/O	H, L	RAM data bus.
72	D4	I/O	H, L	RAM data bus.
73	D5	I/O	H, L	RAM data bus.
74	D6	I/O	H, L	RAM data bus.
75	VSS			Connect to GND.
76	D7	I/O	H, L	RAM data bus.
77	ERR	I/O	H, L	Data input/output pin to C2PO exclusive RAM.
78	EXTC2R	I		C2PO exclusive RAM selection. When used: "H". When not used: "L".
79	BUSY	O	H, L	RAM access busy output. "H": RAM is accessed.

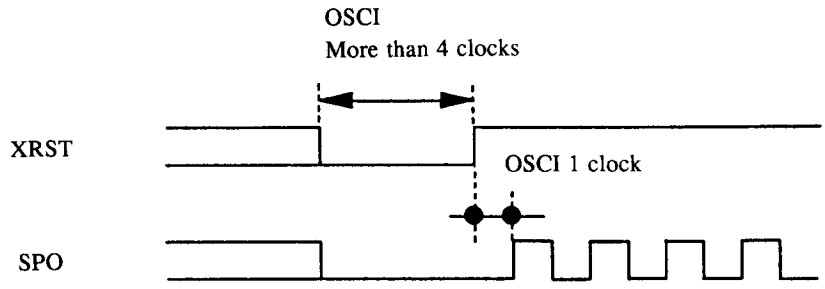
Pin No.	Pin Name	I/O		Function
80	EMP	O	H, L	Outputs signal which indicates ATRAC data empty or just before full.
81	FUL	O	H, L	Outputs signal which indicates ATRAC data full or just before empty.
82	EQL	O	H, L	ATRAC data empty (When ASC = DSC: "H")
83	MDLK	O	H, L	Indicates recorded/played back data main/sub. When "H": Sub or linking. When "L": Main.
84	CPSY	O	H, L	Interpolation sync output.
85	CTMD0	O	H, L	Internal counter mode output.
86	CTMD1	O	H, L	Internal counter mode output.
87	SPO	O	H, L	512 Fs output.
88	VSS			Connect to GND.
89	MDSY	O		Main data sync detection output.
90	LRCK	I		Inputs LRCK (Fs) from the EFM encoder/decoder.
91	BCK	I		Inputs BCK (64 Fs) from the EFM encoder/decoder.
92	C2PO	I		Inputs C2PO from the EFM encoder/decoder.
93	DATA	I/O	H, L	Inputs/outputs data from the EFM encoder/decoder.
94	DIDT	I		Digital recording input pin.
95	DODT	O	H, L	REC monitor output/decode audio data output.
96	DIRCPB	O	H, L	Outputs recording/playback mode to the EFM encoder/decoder. When "H": Recording mode. When "L": Playback mode.
97	MIN	I		External monitor signal input pin.
98	SPOSL	I		SPO input/output selection (L:Input, H:Output)
99	MCK	O		RAM controller internal master clock input
100	VSS			Connect to GND.

- A feedback resistor is incorporated between the OSCI and OSCO pins.
- When the C2PO dedicated RAM is not used (EXT2CR = "L"), open the ERR pin.
- When the XRST pin is "L" (reset), the SPO pin stops the 512 Fs output and becomes "L".

Reset timing when power is on

When the power is turned on and when more than 4 master clocks have been input to the OSCI pin, the XRST pin becomes "H" from "L".

Note) To reset, when the XRST pin is "L", it is necessary to input more than 4 master clocks to the OSCI pin.

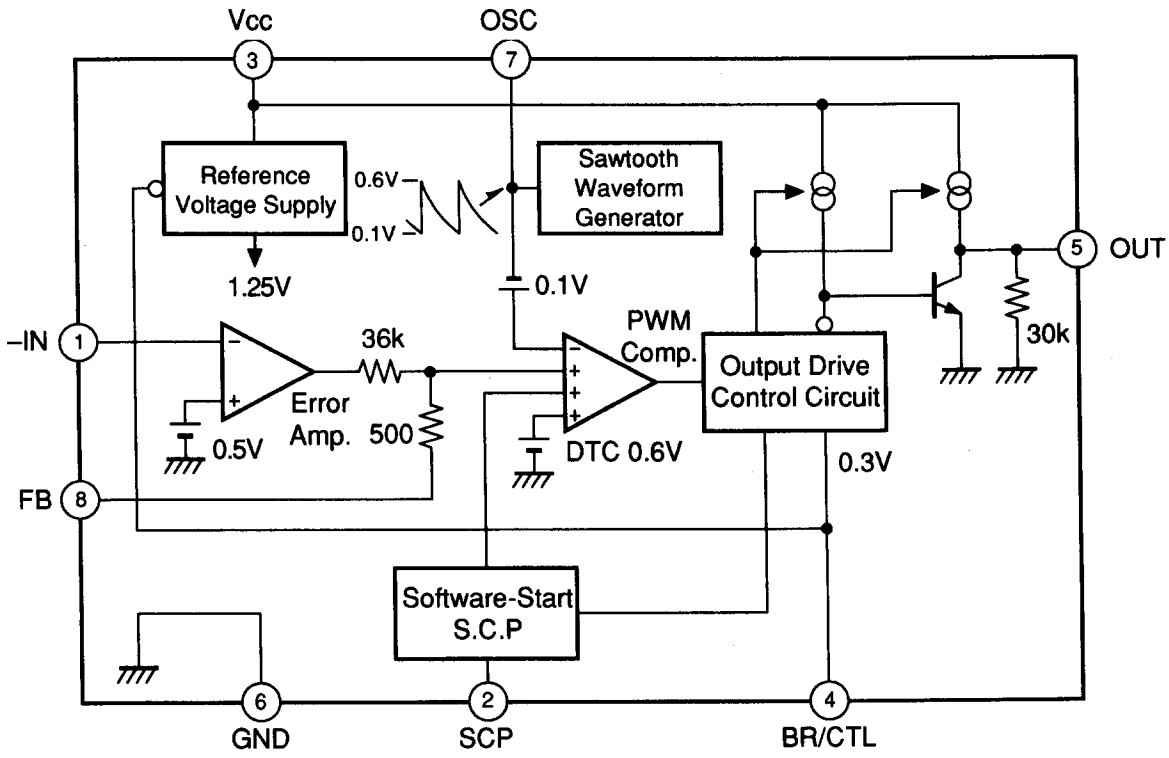


5. Switching Regulator Controller (IC921, MB3800)

(1) Outline

The MB3800 is a low-voltage 1ch switching regulator control IC with the software-start function and short-circuit detection function. With a minimum operation voltage of 1.8V, it is an optimum power supply for battery driven electronic equipment.

(2) Block Diagram



(3) Pin Functions

No.	Pin Name	I/O	Function
1	-IN	I	Error amplifier reverse input terminal
2	SCP	—	Software-start, SCP setting capacity connection terminal
3	Vcc	—	Power supply terminal
4	BR/CTL	I	Output current setting, control terminal
5	OUT	O	Totem pole type output terminal
6	GND	—	GND terminal
7	OSC	—	Oscillation frequency setting capacity and resistance connection terminal
8	FB	O	Error amplifier output terminal

(4) Functions

(i) Switching regulator function

(a) Reference voltage circuit

The reference voltage circuit generates a reference voltage (approx. 1.25V) temperature-compensated by the voltage supplied from the power supply terminal (Pin 3), which is used for setting stop periods, in addition to the reference voltage of the switching regulator.

(b) Sawtooth waveform wave generator

By connecting the capacitor and resistance for setting the oscillation frequency to the OSC terminal (Pin 7), a sawtooth waveform of maximum 1 MHz which is stable against the change in the power supply voltage and a temperature.

(c) Error amplifier

The error amplifier detects the switching regulator output voltage and outputs the PWM control signal. The voltage gain is fixed. By connecting the phase compensation capacitor to the FB terminal (Pin 8), a stable phase compensation can be performed for the system.

(d) PWM comparator

A voltage comparator with one inversion input and three non-inversion inputs. It converts voltages into pulse-width which control the output pulse ON time according to the input voltage. It sets the output level to H when the sawtooth waveform is less than all of the error amplifier output voltage, software-start setting voltage, and stop period setting voltage.

(e) Output circuit

The output circuit is formed in a totem pole type and is able to directly drive the external NPN transistor. The ON/OFF current value can be set by the resistor connected to the BR/CTL terminal (Pin 4).

(ii) Power supply control function

By opening the BR/CTL terminal (Pin 4) or connecting to Vcc, it can be set to the standby state (Power supply current is below 1μA).

(iii) Other Functions

(a) Software-start, Short-circuit detection section

By connecting the C_{PE} to SCP terminal (Pin 2), software-start operations for preventing rush currents during start-up can be set.

After the power supply is connected, charging of the capacitor (C_{PE}) connected to the SCP terminal is started. The software-start setting voltage proportionate to the SCP terminal voltage is compared with the sawtooth waveform by the PWM comparator, the ON duty of the OUT terminal is changed, and software-start operations are performed.

Software-start time (Time required for output ON duty 50%):

$$ts\ [s]=0.35 \times C_{PE}\ [\mu F]$$

After software-start operations end, the SCP terminal (Pin 2) is maintained at L and short-circuit standby state is set.

When the switching regulator output falls suddenly due to load fluctuations, the error amplifier output is fixed at V_{OM^+} charging of the capacitor C_{PE} is started, and when it is charged to about 0.8V, the output terminal (Pin 5) is fixed at L, and at the same time, the SCP terminal (Pin 2) is maintained at L.

When the protection circuit operates, it can be recovered by resetting the power supply.

(b) Low input voltage error operation prevention circuit

In the transient condition of power turning or when the power supply voltage drops instantaneously, errors in the control IC operations result, and the system becomes damaged or deteriorates. The low input voltage error operations prevention circuit compares the power supply voltage with the internal reference voltage for detection, and fixes the output terminal at L.

The power is recovered when the power supply voltage exceeds the threshold voltage of the low input voltage error operation prevention circuit.

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